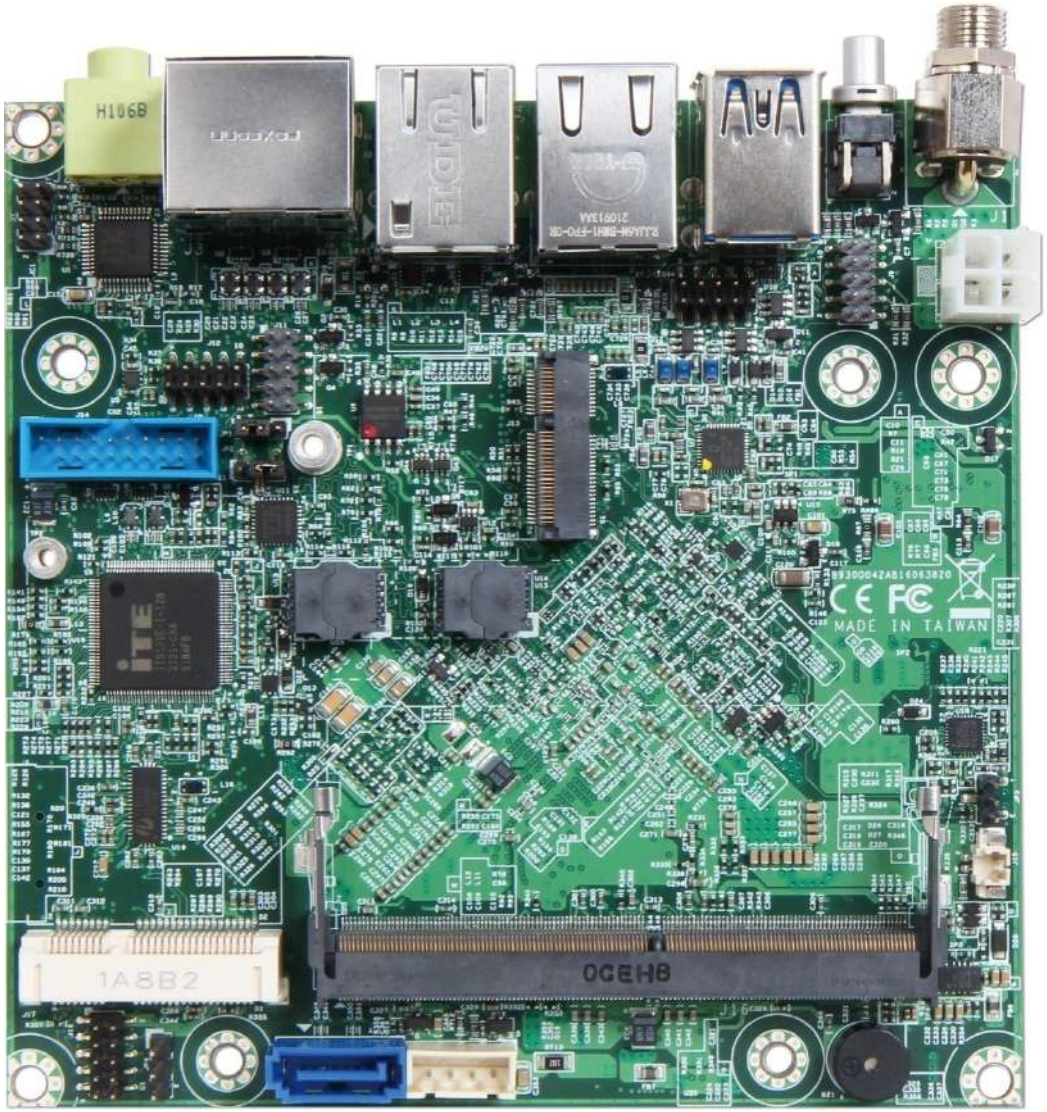
NANO-6063

NANO-ITX EmbeddedBoard

Version 1.0



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Revision History

R1.0	Official Release Rev. 1.0

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Preface

This user's guide provides information about the components, features, connectors and BIOS Setup menus available on the NANO-6063. This document should be referred to when designing NANO-ITX application. The other reference documents that should be used include the following:

- ✧ Intel Elkhart Lake Design Guide
- ✧ Intel Elkhart Lake l Specification

Please contact Portwell Sales Representative for above documents.

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1 Introduction

NANO-6063 utilizing the NANO-ITX formfactor based on the Intel Atom® processor x6000E series.NANO-6063 supports one DDR4SO-DIMM socket up to 32GB and comes with one SATA III, one Mini-PCIe/mSATA socket, one M.2 E key socket, triple display by VGA, DP and HDMI, one GbE, one 2.5GbE, one SD socket and four USB 3.2 Gen2 ports. The NANO-6063 can provide the low powerconsumption for low profile fanless applications such as POS, Print Imaging, ATM,Kiosk, Medical, Panel PC, Digital Security and Digital Signage.

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2 Specifications

Main Processor	◆ Intel Atom® Dual/Quad Core x6000E series Processor
System BIOS	◆ AMI UEFI BIOS
Main Memory	◆ Up to 32 GB in 1 slots DDR4SO-DIMM sockets. ◆ Supports DDR43200MT/s
Graphics	◆ Controller: Intel®Gen 11 Graphics ◆ HDMI: Supports HDMI up to resolution 4096 x 2160@60Hz ◆ DP: Supports DP up to resolution 4096 x 2160@60Hz ◆ VGA: Supports VGA up to resolution 1920 x 1200
Expansion Interface	◆ One M.2 E key(2230) socket for wireless application(PCIe x1 / USD2.0)\ ◆ One full size Mini-PCIe slot(Switch mSATA or Mini-PCIe by BIOS)
SATA Interface	◆ One SATA port(SATA 6Gb/s) ◆ One mSATA socket (Switch mSATA or Mini-PCIe by BIOS)
Input/Output	◆ Serial Port: 1x RS-232/422/485, switched by BIOS ◆ USB Port: 2x USB 3.2 Gen2(type A) on REAR I/O,2x USB 3.2 Gen2 on board header ◆ Audio Interface: Audio jack on rear I/O (Line-out) and on-board pin header (Line-in,Line- out, Mic-in)
Ethernet	◆ Supportsone 10/100/1000 Mbps Ethernet portvia PCI Express x1 (Controller: I210IT) ◆ Supportsone 10/100/1000/2500 Mbps Ethernet portvia SGMII (PHY: GPY215) Note: GPY215 port default supports 1000Mbps. On Elkhart Lake platform, GPY215 cannot automatically downgrade to 10/100/1000 Mbps while setting speed to 2500Mbps
High Drive GPIO	◆ One pin-header for GPIO(8bit in / out)

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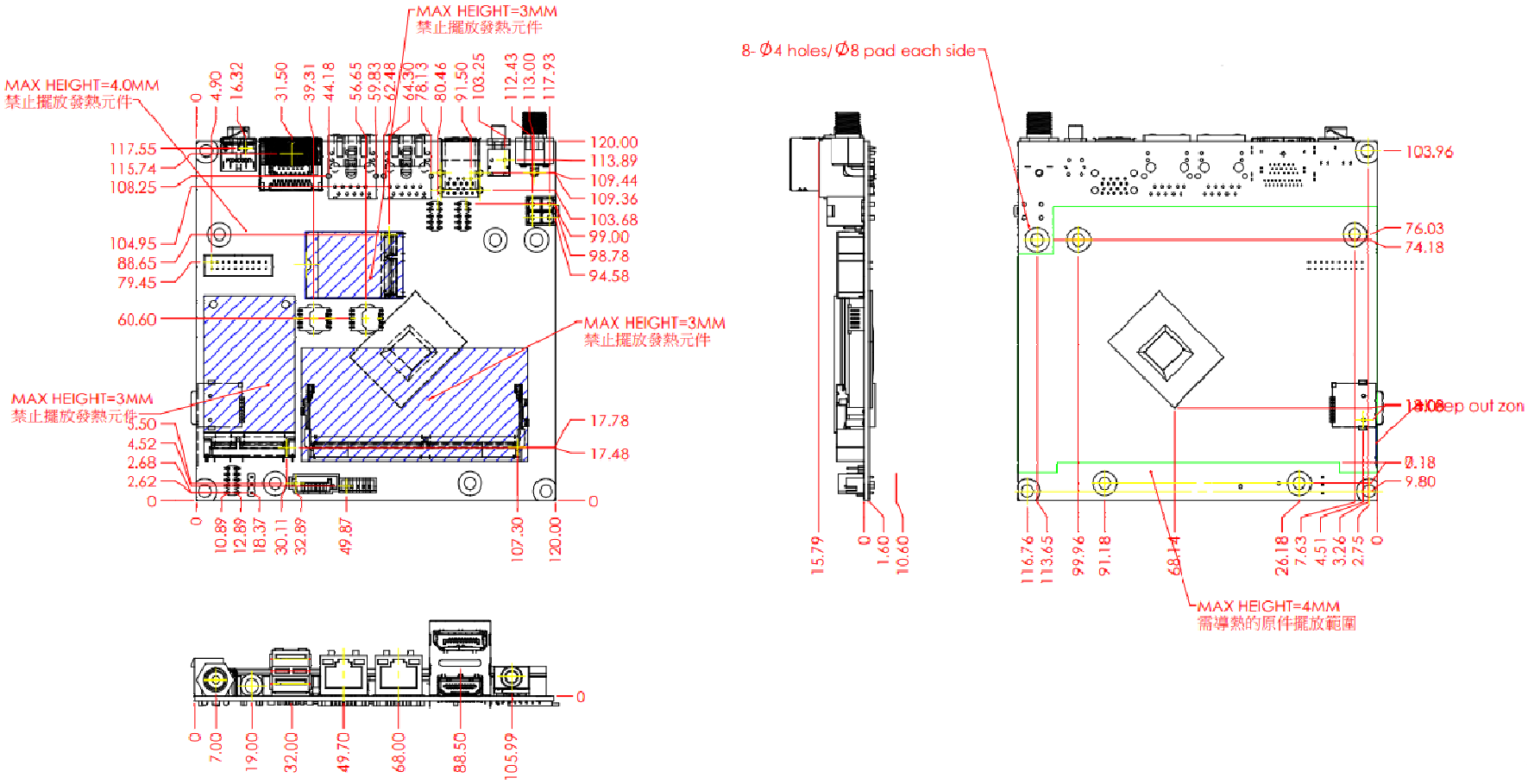
Mechanical and environmental specifications	◆ Operating temperature: -40 ~ 85° C ◆ Storage temperature:-20 ~ 80° C ◆ Humidity: 5 ~ 90% non-condensing ◆ Power supply voltage: 12V DC in ◆ Board size: 120mm x 120 mm (4.72" x 4.72")
EMI/ESD	◆ ESD: IEC 61000-4-2:2008 ◆ EMI: EN 55022: 2010/ AC:2011 Class A

2.1 Supported Operating Systems

The NANO-6063 supports the following operating systems.

- ✧ Windows* 10 IoT Enterprise LTSC 2019, 2021(64bit)
- ✧ Yocto* YP 3.0 Zeus (64 bit)
- ✧ Linux*Kernel version 5.4 (64 bit)

2.2 Mechanical Dimensions



2.3 Power Consumption

Test Configuration	
CPU Type	Intel Atom® x6425RE Processor @ 1.90GHz
SBC BIOS	Portwell, Inc. NANO-6063 BIOS Rev.: 0.0.7 (08102021)
Memory	WARIS DDR4W SO-DIMM 2400 / 8GB *1 (Micron 71B75D9TGX)
Graphic Card	Onboard Intel(R) UHD Graphics
Graphic Driver	Intel(R) UHD Graphics, Version: 27.20.100.8816
LAN Card #1	Onboard Intel(R) I210 Gigabit Network Connection
LAN Driver #1	Intel(R) I210 Gigabit Network Connection, Version: 12.18.11.1
LAN Card #2	Onboard Intel(R) EC1000S 1.0GbE Connection
LAN Driver #2	Intel(R) EC1000S 1.0GbE Connection, Version: 5.123.21.226
Audio Card	Onboard Realtek High Definition Audio
Audio Driver	Realtek High Definition Audio, Version: 6.0.1.6039
Chip Driver	Intel(R) Chipset Device Software, Version: 10.1.18536.8242
USB3.1 Driver	Intel(R) USB 3.10 eXtensible Host Controller – 1.20 (Microsoft), Version: 10.0.19041.1081
EC Version	0.10 (08/06/2021)
Hard Drive	WD5002ABYS
Power Supply	AC/DC Adapter FSP120-AHAN1
Micro SD Card	Kingston SDCA3/16GB 94798-E02.A00LF
mSATA Card	crucial 120GB SATA 6Gb/s SSD (CT120M500SSD3)
Mini-PCIe Card	Mini-PCIe to USB Card, Intel® Dual Band Wireless-AC 7260 (7260HMW)
M.2 Card	Intel® Dual Band Wireless-AC 7265 (7265NGW)

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Power consumption(12V)		
Item	*PowerON*	*Full Loading 10Min*
CPU +12V	3.1 A	2.0 A
CPU +Device +12V	5.1 A	2.1 A
USB Loading Test Port J6 up	4.91 V/ 1.07A	
USB Loading Test Port J6 down	4.91 V/ 1.06A	
USB Loading Test Port J14 left	4.84 V/ 1.03A	
USB Loading Test Port J14 right	4.84 V/ 1.09A	
Full USB port Loading Test (X4)	4.87 V/ 1.06A	

2.4 Environmental Specifications

Storage Temperature : -40~85°C

Operation Temperature : -40~85°C

Storage Humidity : 5~95%, non-condensing

Operation Humidity: 5~95%, non-condensing

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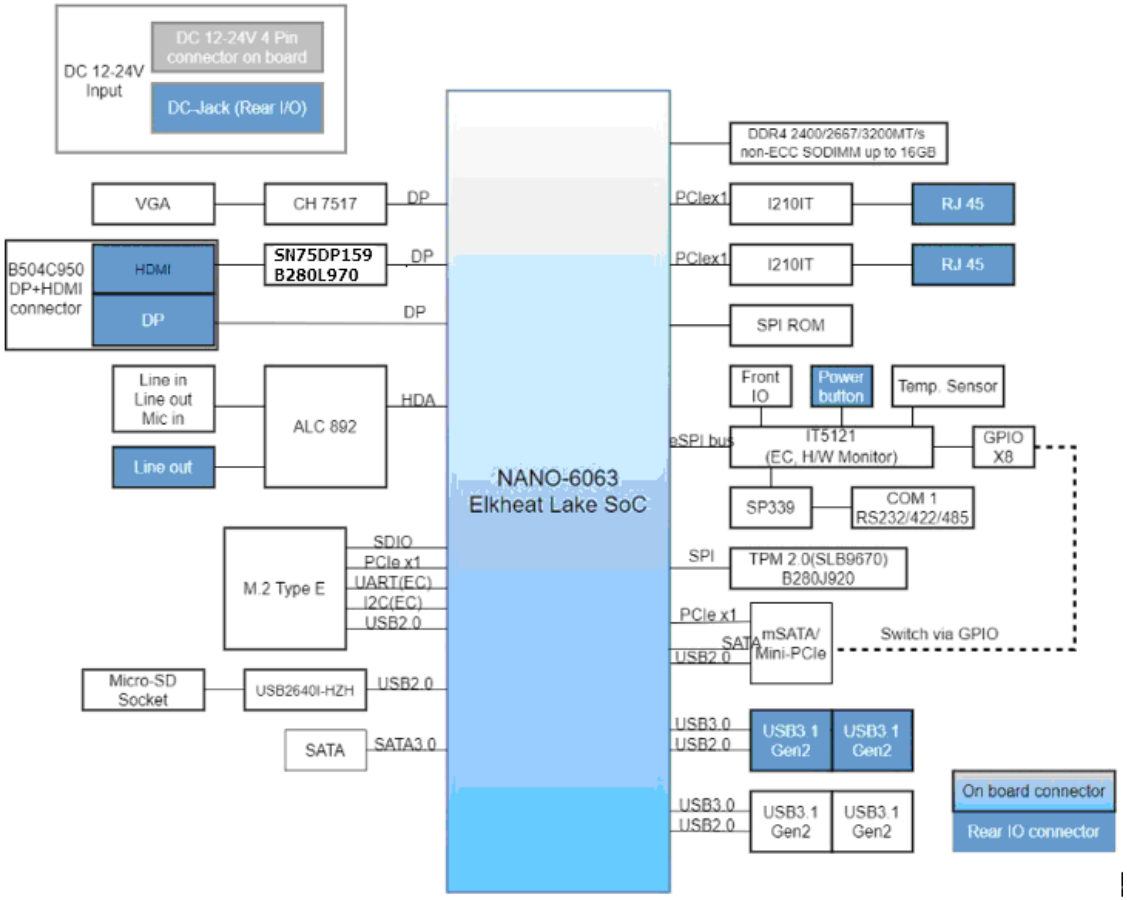
3 Block Diagram



4 Hardware Configuration

4.1 Jumpers and Connectors

Figure 1,NANO-6063 Top View

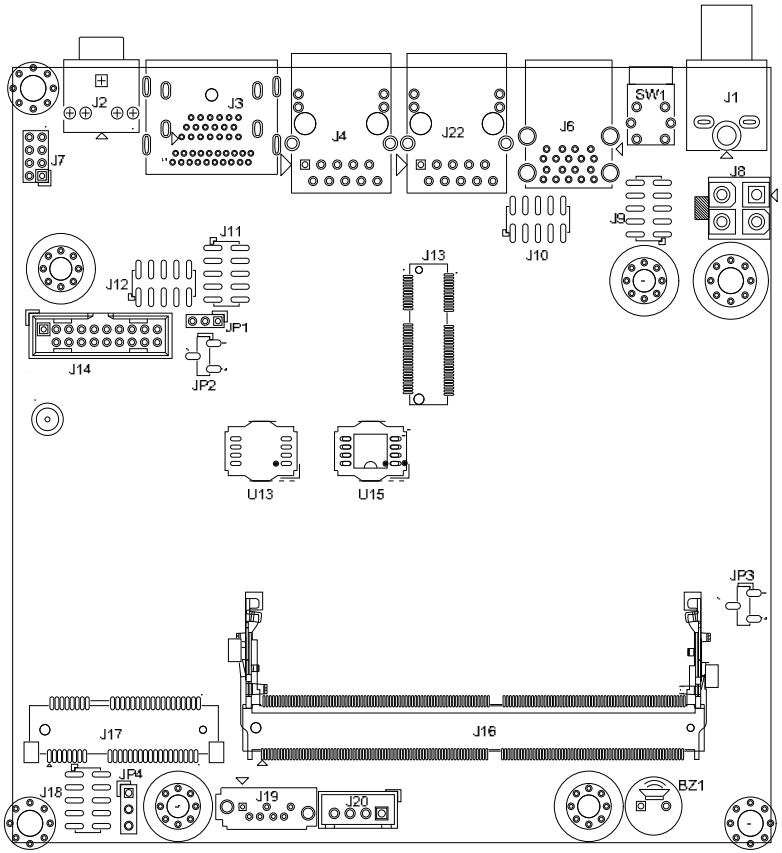
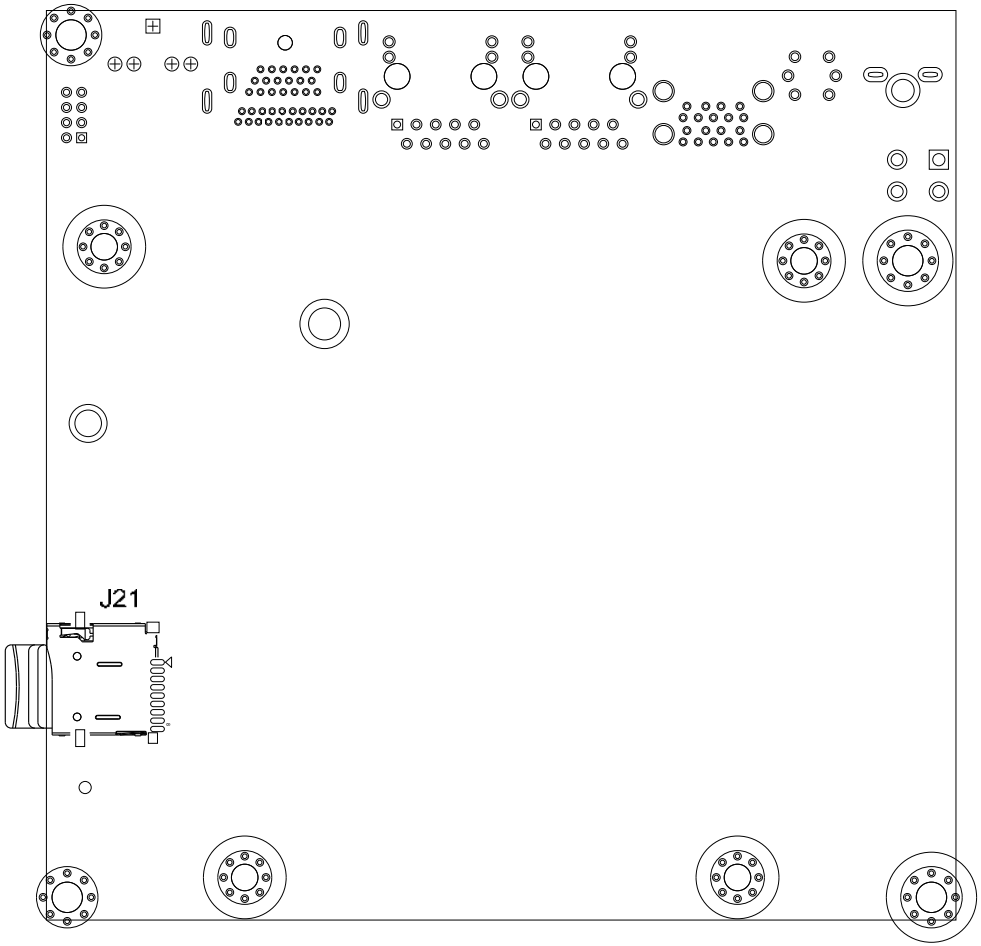


Figure 2,NANO-6063 Bottom View



This chapter indicates jumpers, headers, and connector's locations. Users may find useful information related to hardware settings in this chapter.

4.2 Jumper Settings

For users to customize NANO-6063's features. In the following sections, **Short** means covering a jumper cap over jumper pins; **Open** or N/C (Not Connected) means removing a jumper cap from jumper pins. Users can refer to Figure 1 for the Jumper allocations.

Jumper Table

The jumper settings are schematically depicted in this manual as follows:

Jump Function List:

Jump	Function	Remark
J1	DC Jack	+12V Input
J2	Audio Jack (Line_out)	
J3	DP++ and HDMI Port	
J4/J22	RJ45 Connector	
J6	USB3 Connector	
J7	External Audio (Mic + Line_in + Line_out)Pin HDR.	4x2 pin header
J8	ATX 4 Pin Connector	+12V Input
J9	Front Panel Pin HDR	5x2 pin header
J10	VGA Pin HDR.	5x2 pin header
J11	General Purpose I/O Pin HDR	5x2 pin header
J12	RS232/422/485 Pin HDR	5x2 pin header
J13	M.2 key E Socket	
J14	External USB3 Connector	
J15	Battery Socket	
J16	DDR4 SO-DIMM Socket	
J17	Msata/mini PCIE Socket	
J18	80 Port Connector	5x2 pin header
J19	SATA GEN3 Connector	
J20	SATA Power Connector	

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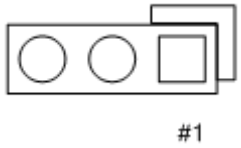
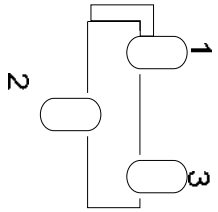
J21	SD Card Socket	
U15	EC Flash	
U13	BIOS Flash	

JP1 : Power On Mode Selection



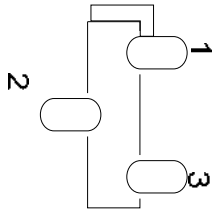
PIN No.	Signal Description
1-2 Short	AT
2-3 Short	ATX ★

JP2 : GPIO4~7 Voltage Output Level Selection



PIN No.	Signal Description
1-2 Short	5V
2-3 Short	3.3V ★

JP3 : CMOS Clear



PIN No.	Signal Description
1-2 Short	Clear CMOS
2-3 Short	n/a

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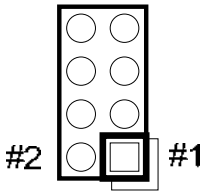
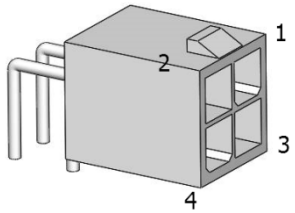
J7 : External Audio Connector



PIN No.	Signal Description	PIN No.	Signal Description
1	MIC_L	2	Line_in_L
3	Ground	4	Line_in_R
5	Line_out_L	6	Ground
7	Line_out_R	8	MIC_R

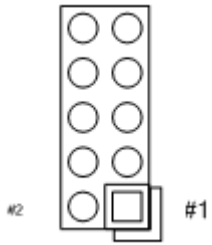
J8 : ATX 4 Pin Connector



PIN No.	Signal Description
1	+12V
2	+12V
3	Ground
4	Ground

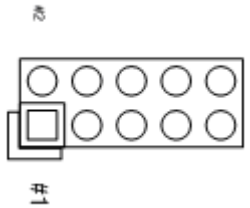
J9 : Front Panel Pin HDR

PIN No.	Signal Description	PIN No.	Signal Description
1	Ground	2	BIOS_RECOVERY



3	External Power LED(+)	4	External Power LED(-)
5	HDD_LED(+)	6	HDD_LED(-)
7	Reset (+)	8	Power On(-)
9	Reset (-)	10	Power On(+)

J10 : VGA Connector



PIN No.	Signal Description	PIN No.	Signal Description
1	RED	2	SCL
3	GREEN	4	GND
5	BLUE	6	SDA
7	VSYNC	8	GND
9	HSYNC	10	+5V

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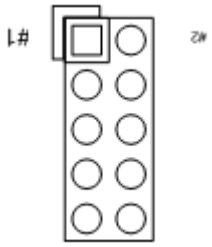
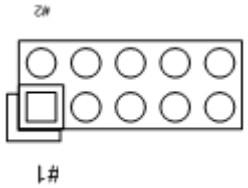
J11: General Purpose I/O Connector



PIN No.	Signal Description	PIN No.	Signal Description
1	GPIO0	2	GPIO4 (Output Only)
3	GPIO1	4	GPIO5 (Output Only)
5	GPIO2	6	GPIO6 (Output Only)
7	GPIO3	8	GPIO7 (Output Only)
9	Ground	10	+5V

J12: RS-232/422/485I/O

Connector



PIN No.	Signal Description	PIN No.	Signal Description
1	DCD#/485D-/422T-	2	RXD#/485D+/422T+
3	TXD#/422R+	4	DTR#/422R-
5	Ground	6	DSR#
7	RTS#	8	CTS#
9	RI#	10	N/C

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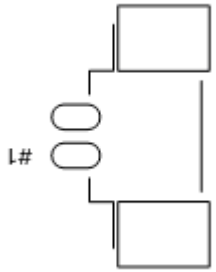
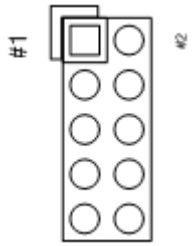
J15 : Battery Connector



PIN No.	Signal Description
1	Battery Voltage
2	Ground

J18 : 80 Port Connector



PIN No.	Signal Description	PIN No.	Signal Description
1	EC_LEDA	2	3.3V
3	EC_LEDB	4	EC_LEDE
5	EC_LEDC	6	EC_LEDF
7	EC_LEDD	8	EC_LEDG
9	EC_DGL#	10	GND

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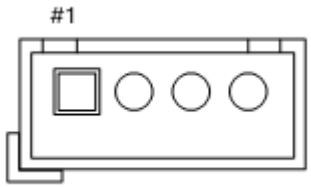
J20 : SATA Power Connector



PIN No.	Signal Description
1	+12V
2	Ground
3	Ground
4	+5V

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5 Signal Descriptions

5.1 Watch Dog Timer

```
#include <stdio.h>
#include <unistd.h>
#include <stdint.h>
#include <sys/io.h>

#define EC_IOSpace 0xE300    // EC IO Space Base Addr = 0xE000
                             // EC Internal Offset = 0x300
                             // EC IO Address = Base Addr + Internal offset

#define WDTCFG               0x06       // WDT Timer Coutrol Register
                             // Bit 6: Write 1 to clear WDT pin event (COMe Only)
                             // Bit 4: 1: Driving WDT pin to Carrier (COMe Only)
                             //        0: System Reset
                             // Bit 1: 1: Min Mode
                             //        0: Second Mode
                             // Bit 0: 1: Enable WDT
#define WDTMIN               0x07       // WDT Timer Counter Register (Minute)
#define WDTSEC               0x08       // WDT Timer Counter Register (Second)

int Read_EC_SRAM(int offset)
```

```
{
        int Temp;
        Temp = inb_p(EC_IOSpace+offset);
        return Temp;
}

void Write_EC_SRAM(int offset, int value)
{
outb_p(value,EC_IOSpace+offset);
}

//---------------------------------
// Reset WDT pin status
//---------------------------------
int WDT_Reset()
{
      int Temp;

      Temp = Read_EC_SRAM(WDTCFG);
Write_EC_SRAM(WDTCFG,(Temp|0x40));    // Bit 6: Write 1 to clear WDT pin event
}

//---------------------------------
// Main Function
//---------------------------------
int main (int argc, char ** argv)
{
```

```
	int Temp;

	// Initial
	if(iopl(3)!=0){
printf("error: I/O Permission Error!\n");
		return 1;
	}

	// Enable WDT 10min, 20sec
Write_EC_SRAM(WDTSEC,5);			// 5 Sec
Write_EC_SRAM(WDTMIN,1);			// 1 min

	// Enable WDT 5sec and WDT pin mode
	Temp = Read_EC_SRAM(WDTCFG);
Write_EC_SRAM(WDTCFG,(Temp|0x13));	// Bit4: 1: Driving WDT pin
						// BIT1: 1: Minute Mode
						// Bit0: 1: Enable WDT
	// Check Current WDT status
	while((Read_EC_SRAM(WDTCFG)&0x01) != 0)
	{
printf("WDT Counting: %d M., %d S!\n",Read_EC_SRAM(WDTMIN),Read_EC_SRAM(WDTSEC));
	}
}
```

5.2 Signal GPIO Signal

```
#include <stdio.h>
#include <unistd.h>
#include <stdint.h>
#include <sys/io.h>

#define EC_IOSpace 0xE300    // EC IO Space Base Addr = 0xE000
                             // EC Internal Offset = 0x300
                             // EC IO Address = IO Space Base Addr + Internal offset

#define GPCR 0x2B        // GPIO Coutrol Register, Bit7 = GPO3, Bit6 = GPO2, ...,
                         //                        Bit3 = GPI3, Bit2 = GPI2, ...,
                         // 0: Output; 1: Input

#define GPDR 0x2C        // GPIO Status Register, Bit7 = GPO3, Bit6 = GPO2, ...,
                         //                       Bit3 = GPI3, Bit2 = GPI2, ...,
                         // 0: Low; 1: High
int Read_EC_SRAM(int offset)
{
        int Temp;
        Temp = inb_p(EC_IOSpace+offset);
        return Temp;
}

void Write_EC_SRAM(int offset, int value)
```

```
{
outb_p(value,EC_IOSpace+offset);
}

int main (int argc, char ** argv)
{
        int Temp;

        // Initial
        if(iopl(3)!=0){
printf("error: I/O Permission Error!\n");
                return 1;
        }
        // Get GPI status
        Temp = Read_EC_SRAM(GPDR);                      //Bit3-0: GPI3-0 status

        // Set GPO4 Output & High
        Temp = Read_EC_SRAM(GPDR);
Write_EC_SRAM(GPDR,Temp|0x80);                  //Bit7-4: Set GPO3-0 status, 0: Low 1: High

        return 0;
}
```

6 BIOS Setup Items

NANO-6063 is equipped with the AMI BIOS stored in Flash ROM. These BIOS has a built-in Setup program that allows users to modify the basic system configuration easily. This type of information is stored in CMOS RAM so that it is retained during power-off periods. When system is turned on, NANO-6063 communicates with peripheral devices and checks its hardware resources against the configuration information stored in the CMOS memory. If any error is detected, or the CMOS parameters need to be initially defined, the diagnostic program will prompt the user to enter the SETUP program. Some errors are significant enough to abort the start up.

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6.1 Entering Setup -- Launch System Setup

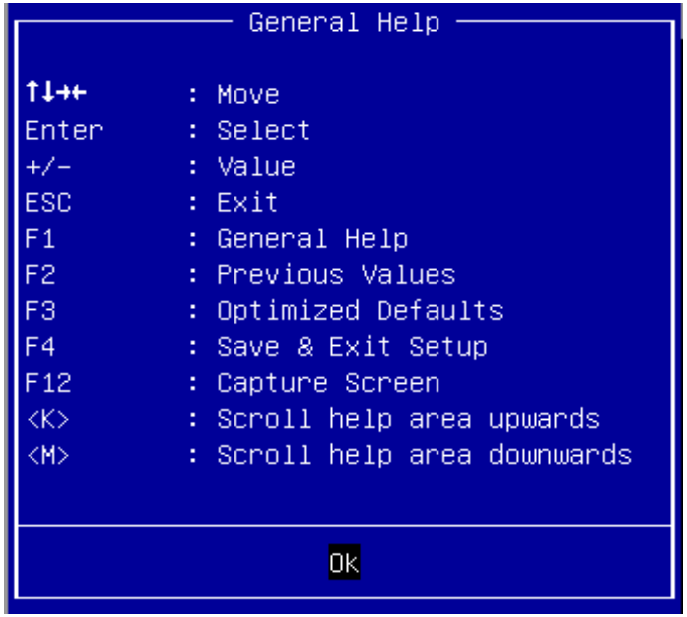
Power on the computer and the system will start POST (Power On Self Test) process. When the message below appears on the screen, press <Del> key will enter BIOS setup screen.

Press <Del> to enter SETUP

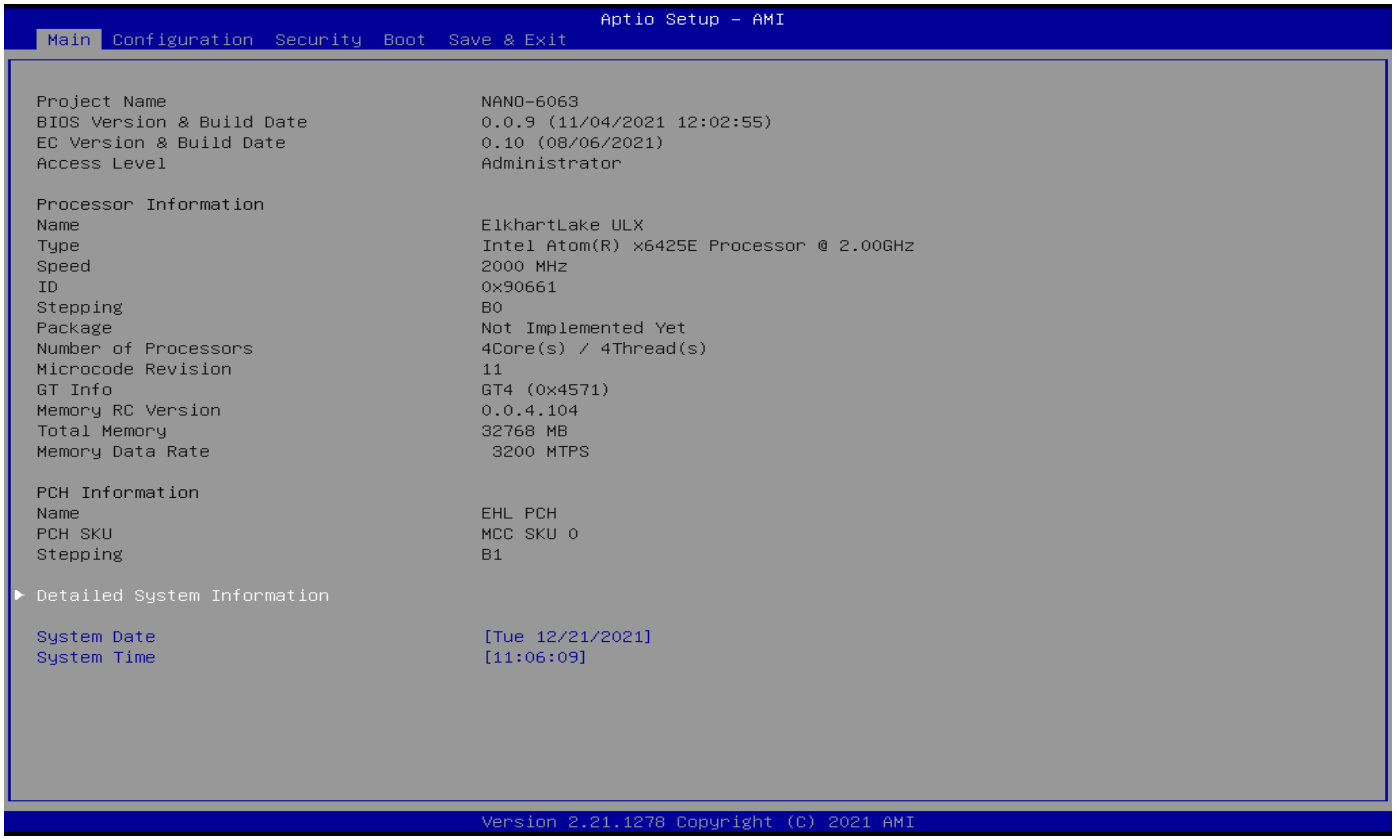
If the message disappears before responding and still wish to enter Setup, please restart the system by turning it OFF and On or pressing the RESET button. It can be also restarted by pressing <Ctrl>, <Alt>, and <Delete> keys on keyboard simultaneously.

Press <F1> to Run General Help or Resume

The BIOS setup program provides a General Help screen. The menu can be easily called up from any menu by pressing <F1>. The Help screen lists all the possible keys to use and the selections for the highlighted item. Press <Esc> to exit the Help screen.

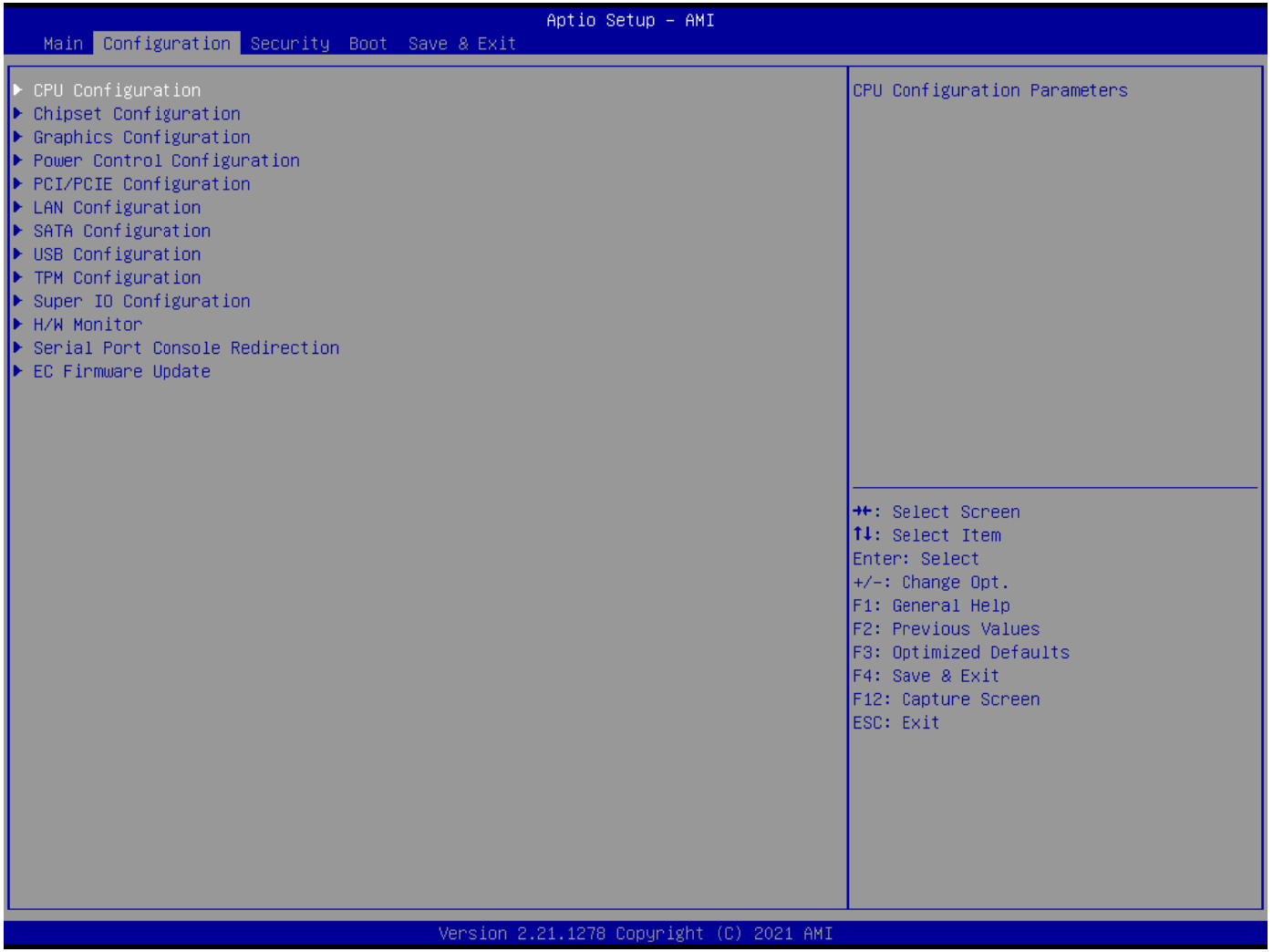


6.2 Main

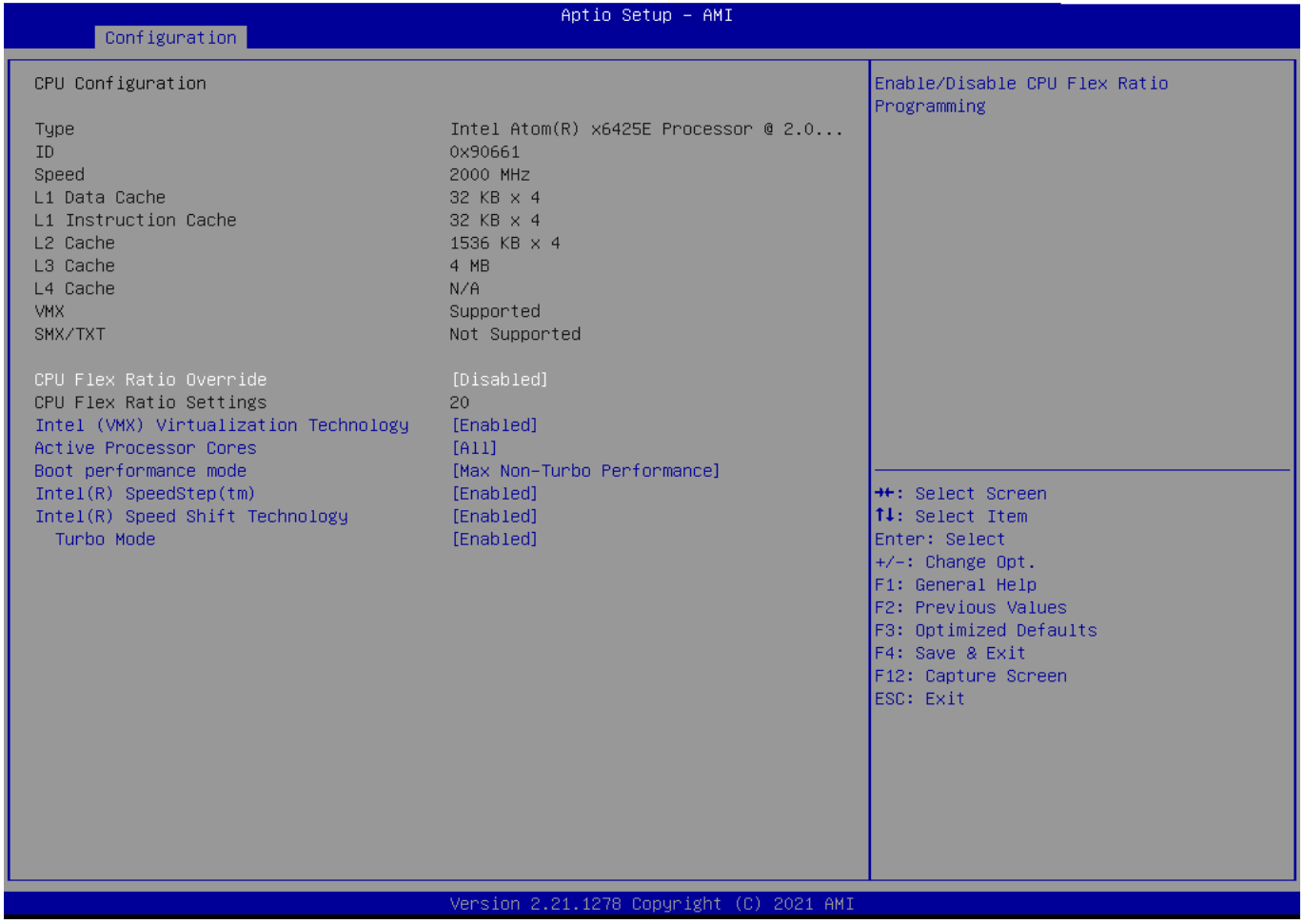


Feature	Description	Options
System Date	The date format is <Day>, <Month> <Date> <Year>. Use [+] or [—] to configure system Date.	
System Time	The time format is <Hour> <Minute> <Second>. Use [+] or [—] to configure system Time.	

6.3 Configuration



CPU Configuration



Feature	Description	Options
CPU Flex Ratio Override	Enable/Disable CPU Flex Ratio Programming	★ Disabled, Enabled
CPU Flex Ratio Settings	This value must be between Max Efficiency Ratio (LFM) and Maximum non-turbo ratio set by Hardware (HFM).	★ 20
Intel (VMX) Virtualization Technology	When enabled, a VMM can utilize the additional hardware capabilities provided by Vander pool Technology.	★ Enabled, Disabled
Active Processor Cores	Number of cores enable in each processor package.	★ All, 1, 2, 3
Boot performance mode	Select the performance state that the BIOS will set starting from reset vector	★ Max Non-Turbo Performance, Max Battery, Turbo Performance,
Intel® SpeedStep™	Allows more than two frequency ranges to be supported.	★ Enabled, Disabled
Intel® Speed Shift Technology	Enable/Disable Intel® Speed Shift Technology support. Enabling will expose the CPPC v2 interface to allow for hardware controlled P-states	★ Enabled, Disabled
Turbo Mode	Enable/Disable processor Turbo Mode (requires EMTTM enabled too). AUTO means enabled.	★ Enabled, Disabled

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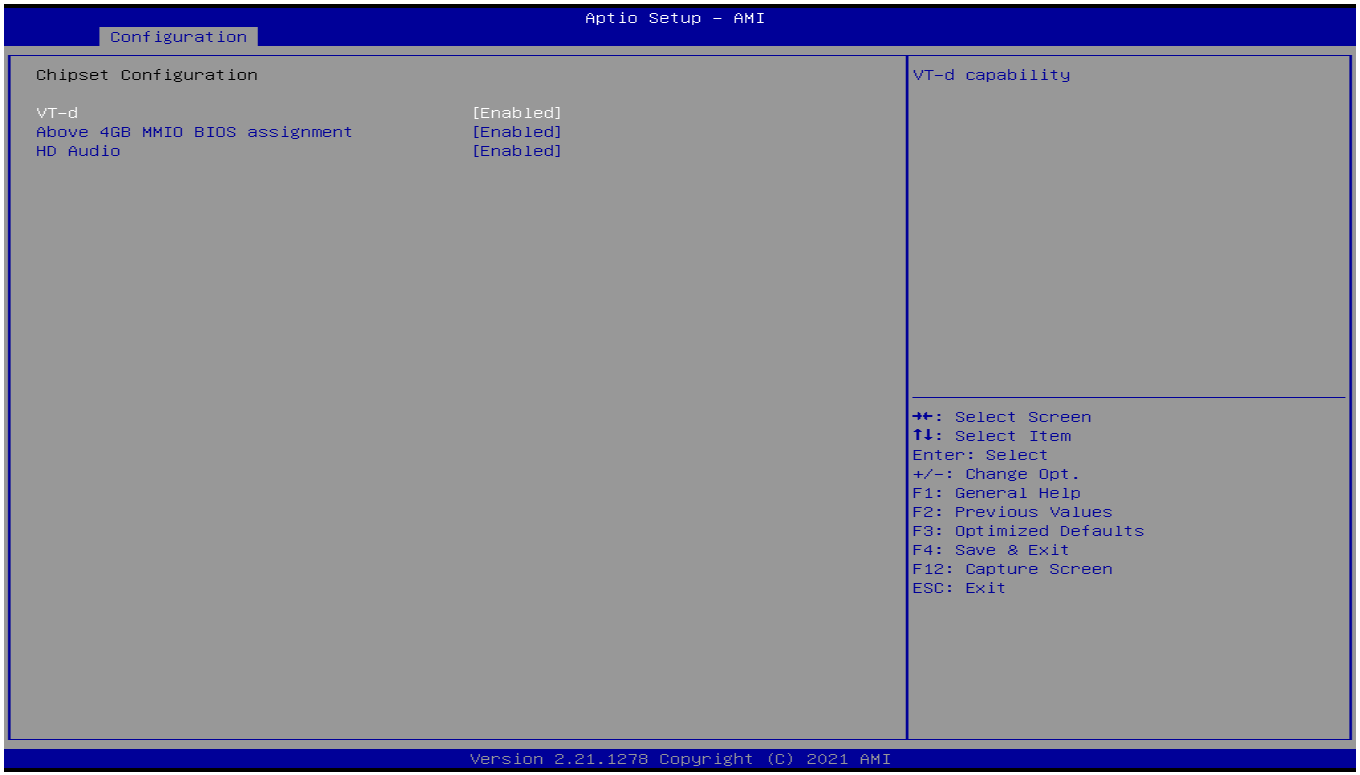
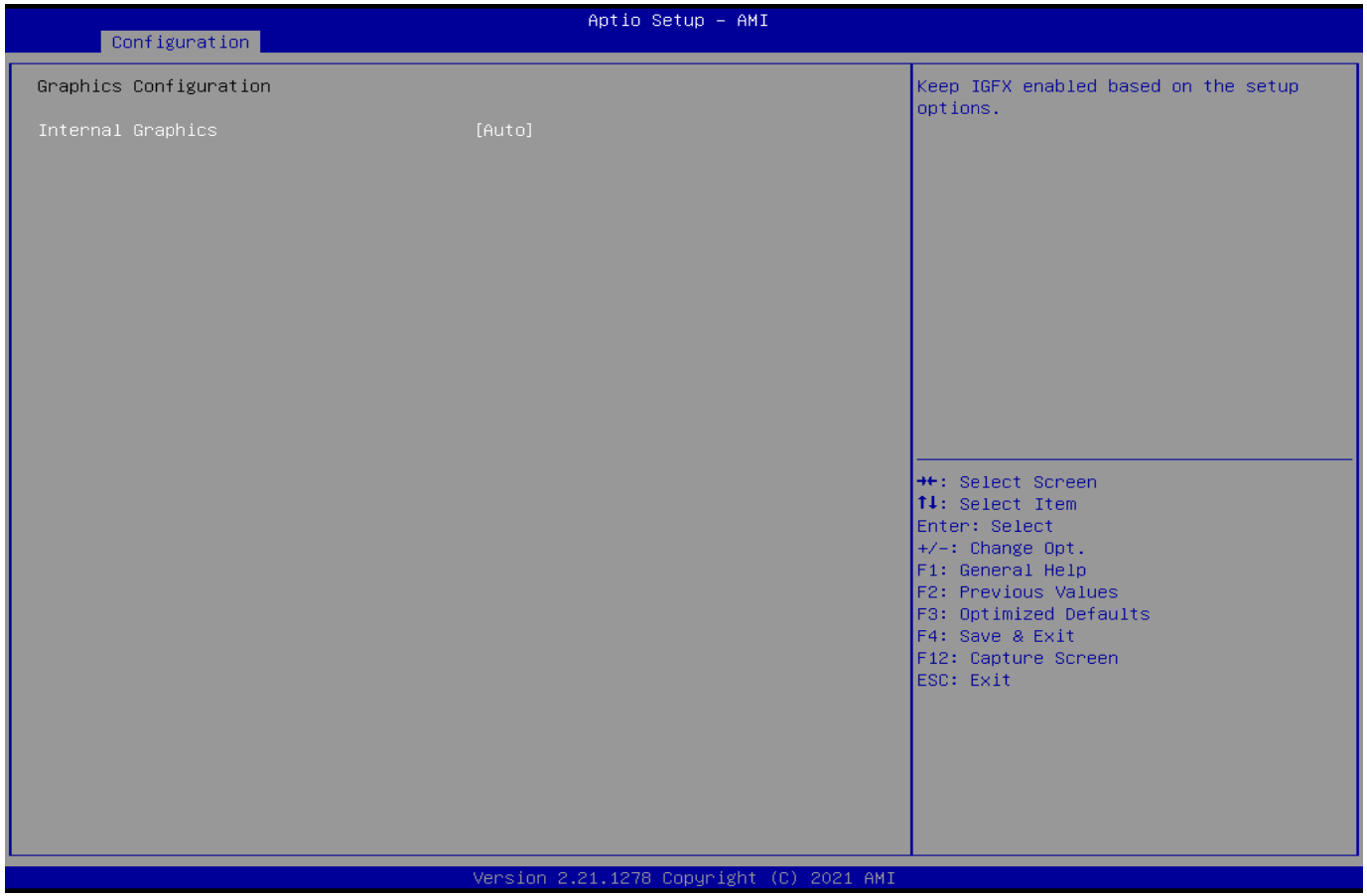
Chipset Configuration



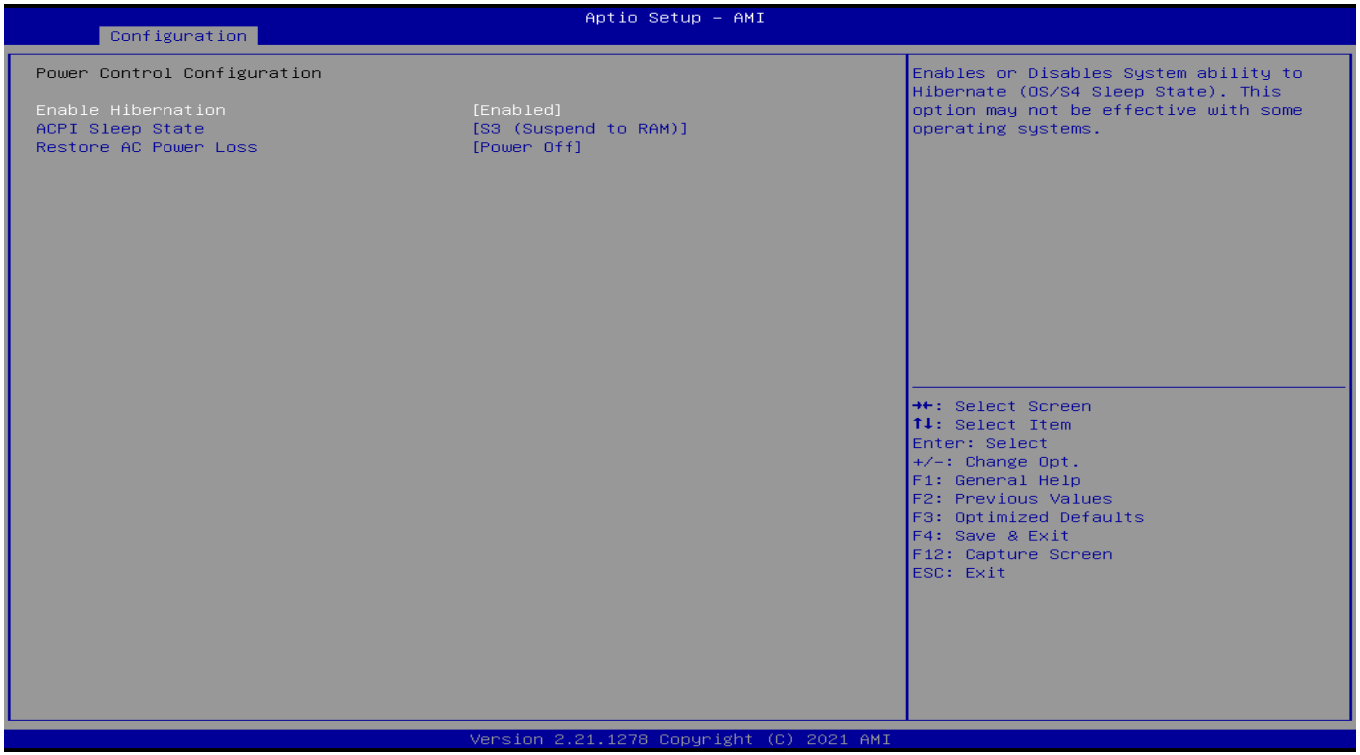
Feature	Description	Options
VT-d	VT-d Capability	★ Enabled ,Disabled
Above 4GB MMIO BIOS assignment	Enable/Disable above 4GB Memory Mapped IO BIOS assignment This is enabled automatically when Aperture Size is set to 2048MB	★ Enabled ,Disabled
HD Audio	Control Detection of the HD-Audio device. Disabled = HAD will be unconditionally disabled Enabled = HAD will be unconditionally enabled	★ Enabled ,Disabled

Graphics Configuration



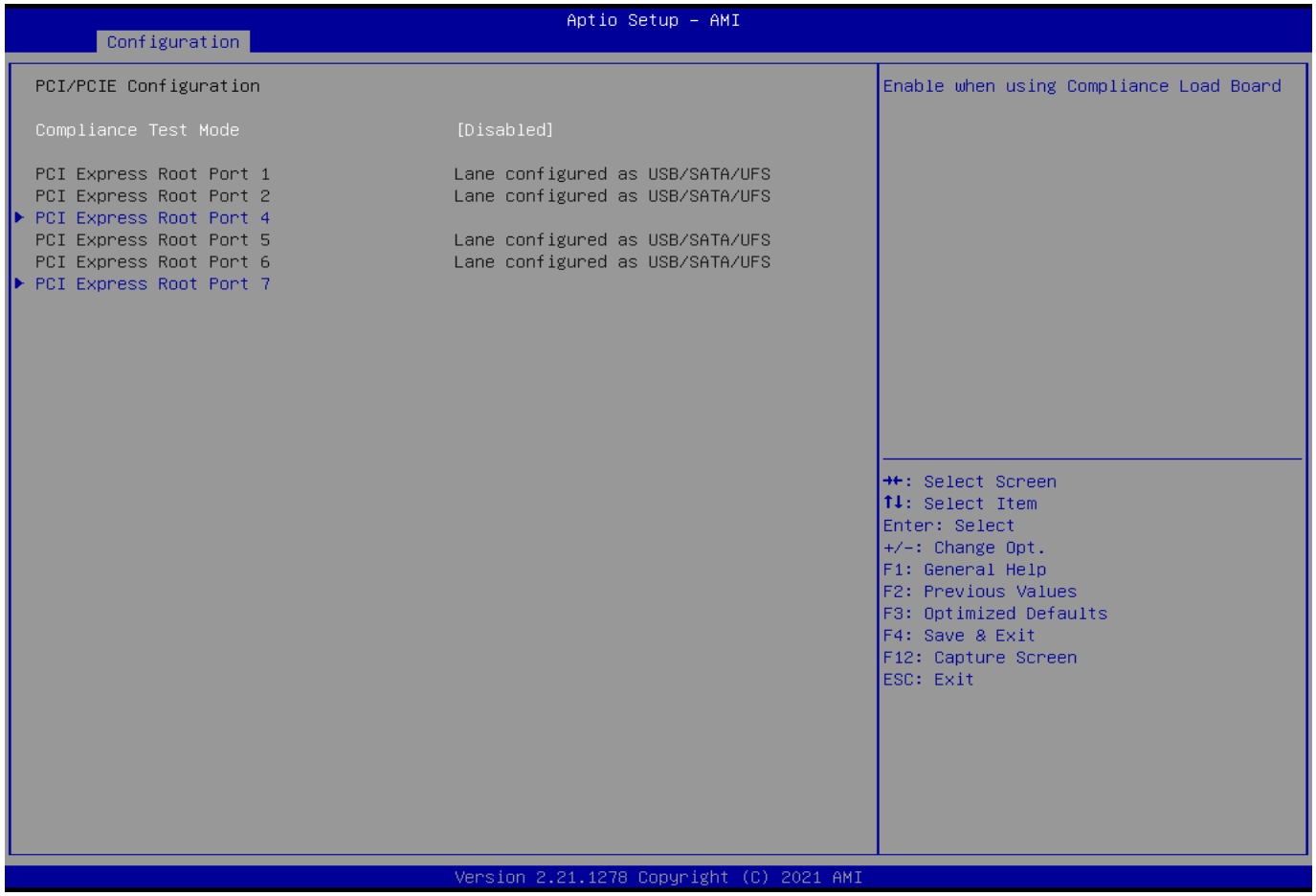
Feature	Description	Options
Internal Graphics	Keep IGFX enabled based on the setup options.	★ Auto, Disabled, Enabled

Power Control Configuration

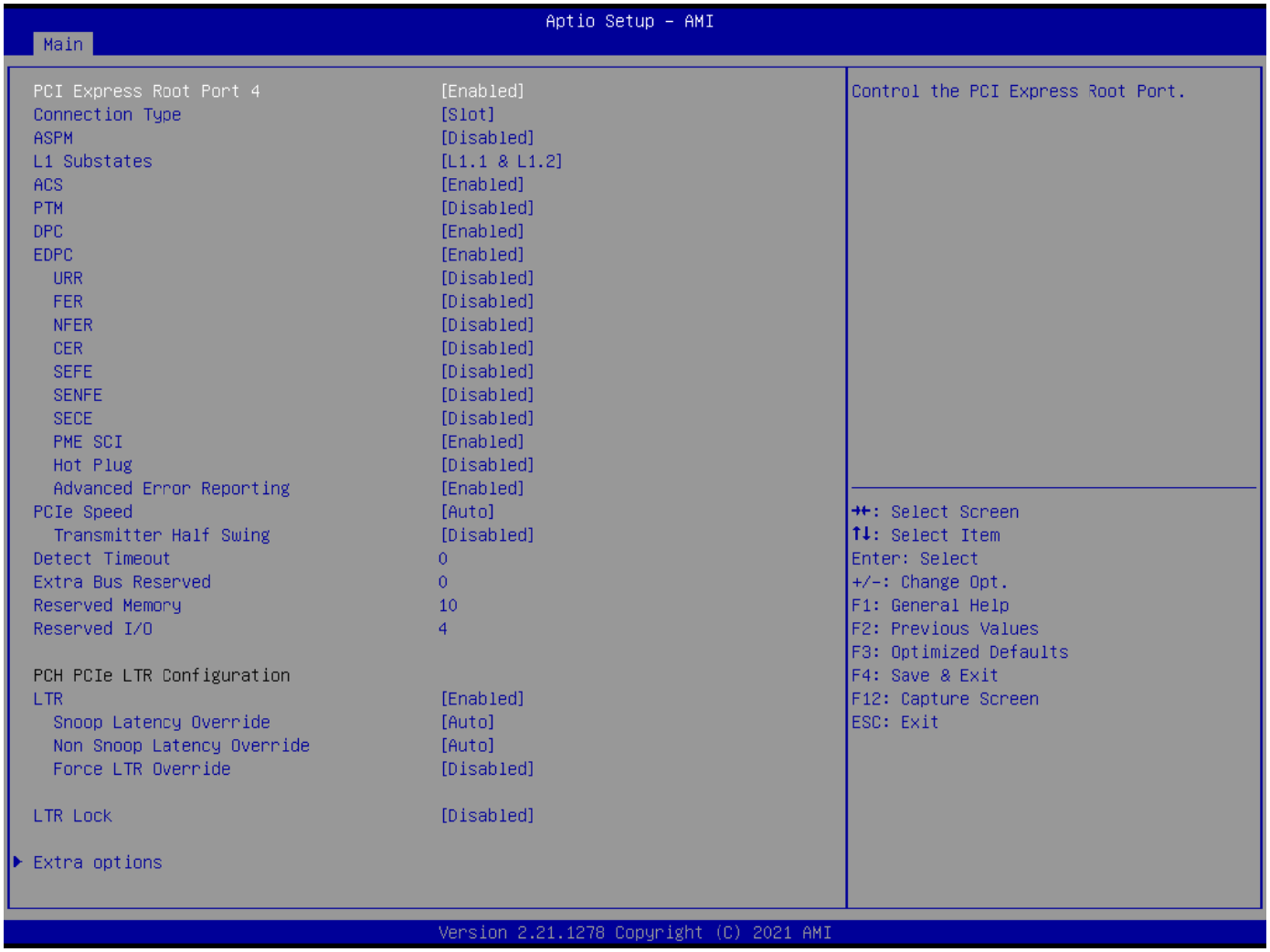


Feature	Description	Options
Enable Hibernation	Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may not be effective with some operating systems.	★ Enabled, Disabled
ACPI Sleep State	Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed.	★ S3 (Suspend to RAM), Suspend Disabled
Restore AC Power Loss	Specify what state to go to when power is re-applied after a power failure (G3 state)	★ Power Off, Power On

PCI/PCIE Configuration



Feature	Description	Options
Enable Hibernation	Enables when using Compliance Load Board.	★ Disabled, Enabled


Aptio Setup – AMI
Main
PCI Express Root Port 4 [Enabled]
Connection Type [Slot]
ASPM [Disabled]
L1 Substates [L1.1 & L1.2]
ACS [Enabled]
PTM [Disabled]
DPC [Enabled]
EDPC [Enabled]
URR [Disabled]
FER [Disabled]
NFER [Disabled]
CER [Disabled]
SEFE [Disabled]
SENFE [Disabled]
SECE [Disabled]
PME SCI [Enabled]
Hot Plug [Disabled]
Advanced Error Reporting [Enabled]
PCIe Speed [Auto]
Transmitter Half Swing [Disabled]
Detect Timeout 0
Extra Bus Reserved 0
Reserved Memory 10
Reserved I/O 4
PCH PCIe LTR Configuration
LTR [Enabled]
Snoop Latency Override [Auto]
Non Snoop Latency Override [Auto]
Force LTR Override [Disabled]
LTR Lock [Disabled]
Extra options
Control the PCI Express Root Port.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
F12: Capture Screen
ESC: Exit
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Feature	Description	Options
COMe PCIe Port	Control the PCI Express Root Port.	★ Enabled , Disabled
Connection Type	Built-In: a built-in device is connected to this root port. Slot Implemented bit will be clear. Slot: this root port connects to user-accessible slot. Slot Implemented bit will be set.	★ Slot, Built-in
ASPM	Set the ASPM Level: Force L0s – Force all links to L0s State AUTO - BIOS auto configure DISABLE – Disables ASPM	★ Disabled, L0s, L1, L0sL1, Auto
L1 Substates	PCI Express L1 Substates settings.	★ L1.1 & L1.2, L1.1, Disabled
ACS	Enable/Disable Access Control Services Extended Capability	★ Enabled , Disabled
PTM	Enable/Disable Precision Time Measurement	★ Disabled, Enabled
DPC	Enable/Disable Downstream Port Containment	★ Enabled , Disabled
EDPC	Enable/Disable Rootport extensions for Downstream Port Containment	★ Enabled , Disabled
URR	PCI Express Unsupported Request Reporting Enable/Disable.	★ Disabled, Enabled
FER	PCI Express Device Fatal Error Reporting Enable/Disable	★ Disabled, Enabled
NFER	PCI Express Device Non-Fatal Error Reporting Enable/Disable	★ Disabled, Enabled
CER	PCI Express Device Correctable Error Reporting Enable/Disable.	★ Disabled, Enabled
SEFE	Root PCI Express System Error on Fatal Error Enable/Disable.	★ Disabled, Enabled
SENFE	Root PCI Express System Error on Non-Fatal Error Enable/Disable.	★ Disabled, Enabled
SECE	Root PCI Express System Error on Correctable Error Enable/Disable.	★ Disabled, Enabled
PME SCI	PCI Express PME SCI Enable/Disable.	★ Enabled , Disabled

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Hot Plug	PCI Express Hot Plug Enable/Disable.	★ Disabled, Enabled
Advanced Error Reporting	Advanced Error Reporting Enable/Disable.	★ Enabled , Disabled
PCIe Speed	Configure PCIe Speed	★ Auto, Gen1, Gen2, Gen3
Transmitter Half Swing	Transmitter Half Swing Enable/Disable.	★ Disabled, Enabled
Detect Timeout	The number of milliseconds reference code will wait for link to exit Detect state for enabled ports before assuming there is no device and potentially disabling the port.	★ 0
Extra Bus Reserved	Extra Bus Reserved (0-7) for bridges behind this Root Bridge.	★ 0
Reserved Memory	Reserved Memory for this Root Bridge (1-20) MB	★ 10
Reserved I/O	Reserved I/O (4K/8K/12K/16K/20K) Range for this Root Bridge.	★ 4
LTR	PCH PCIE Latency Reporting Enable/Disable	★ Enabled , Disabled
Snoop Latency Override	Snoop Latency Override for PCH PCIE. Disabled: Disable override. Manual: Manually enter override values. Auto (default): Maintain default BIOS flow.	★ Auto, Manual, Disabled
Snoop Latency Value	LTR Snoop Latency value of PCH PCIE	★ 60
Snoop Latency Multiplier	LTR Snoop Latency Multiplier of PCH PCIE	★ 1024ns, 1ns, 32ns, 32768ns, 1048576ns, 33554432ns
Non Snoop Latency Override	Non Snoop Latency Override for PCH PCIE. Disabled: Disable override. Manual: Manually enter override values. Auto (default): Maintain default BIOS flow.	★ Auto, Manual, Disabled
Non Snoop Latency Value	LTR Non Snoop Latency value of PCH PCIE	★ 60

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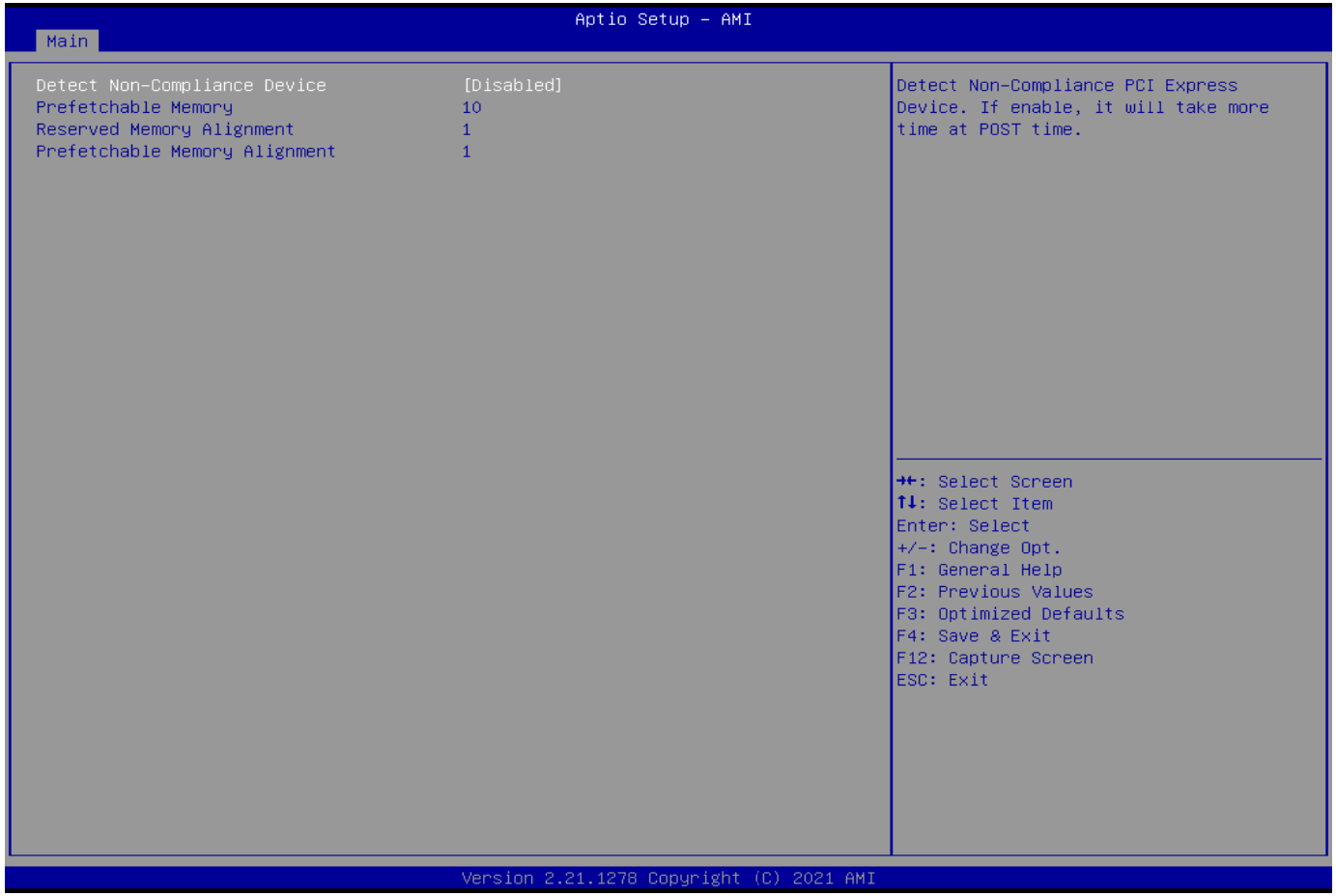
Non Snoop Latency Multiplier	LTR Non Snoop Latency Multiplier of PCH PCIE.	★ 1024ns, 1ns, 32ns, 32768ns, 1048576ns, 33554432ns
Force LTR Override	Force LTR Override for PCH PCIE. Disabled: LTR override values will not be forced. Enable: LTR override values will be forced and LTR messages from the device will be ignored.	★ Disabled, Enabled
LTR Lock	PCIE LTR Configuration Lock	★ Disabled, Enabled
Extra options	PCI Express Root Port extra options.	

Extra options



Feature	Description	Options
Detect Non-Compliance Device	Detect Non-Compliance PCI Express Device. If enable, it will take more time at POST time.	★ Disabled, Enabled
Prefetchable Memory	Prefetchable Memory Range for this Root Bridge.	★ 10
Reserved Memory Alignment	Reserved Memory Alignment (0 – 31 bits)	★ 1
Prefetchable Memory Alignment	Prefetchable Memory Alighnment (0 – 31 bits)	★ 1

LAN Configuration

Feature	Description	Options
Intel PSE TSN GbE #0 (SGMII Mode)		
PSE TSN GBE 0	Select ownership for GBE	★ Host owned with pin muxed, SPE owned with pin muxed, None
PSE TSN GBE 0 Link Speed	PSE TSN GBE 0 Link Speed configuration.	★ SGMII 1 Gbps, SGMII 2.5 Gbps
Intel Ethernet Controller WGI210AT		
On Board LAN	Controller On Board LAN Enabled or Disabled	★ Enabled , Disabled
On Board USB Power		
USB Port 0/1 Power	Controller USB Port Power Enabled or Disabled	★ Enabled , Disabled
USB Port 2/3 Power	Controller USB Port Power Enabled or Disabled	★ Enabled , Disabled
Network Stack (Enabled)		
IPv4 PXE Support	Enable/Disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support Will not be available.	★ Enabled , Disabled
IPv4 HTTP Support	Enable/Disable IPv4 HTTP boot support. If disabled, IPv4 HTTP boot support Will not be available.	★ Enabled , Disabled
IPv6 PXE Support	Enable/Disable IPv6 PXE boot support. If disabled, IPv6 PXE boot support Will not be available.	★ Enabled , Disabled
IPv6 HTTP Support	Enable/Disable IPv6 HTTP boot support. If disabled, IPv6 HTTP boot support Will not be available.	★ Enabled , Disabled
PXE boot wait time	Wait time in seconds to press ESC key to abort the PXE boot. Use either +/- or numeric keys to set the value.	★ 0
Media detect count	Number of times the presence of media will be checked. Use either +/- or numeric keys to set the value.	★ 1

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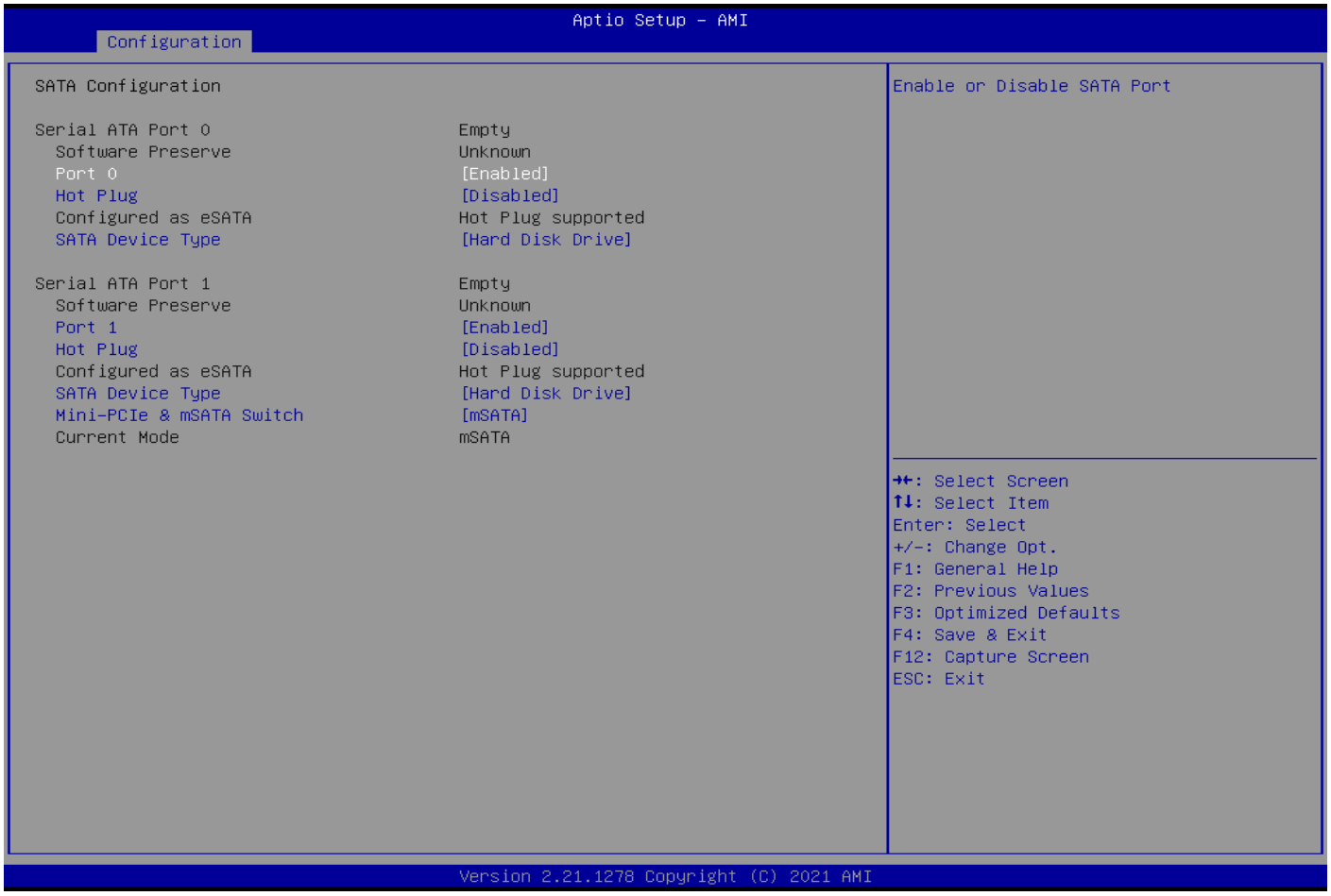
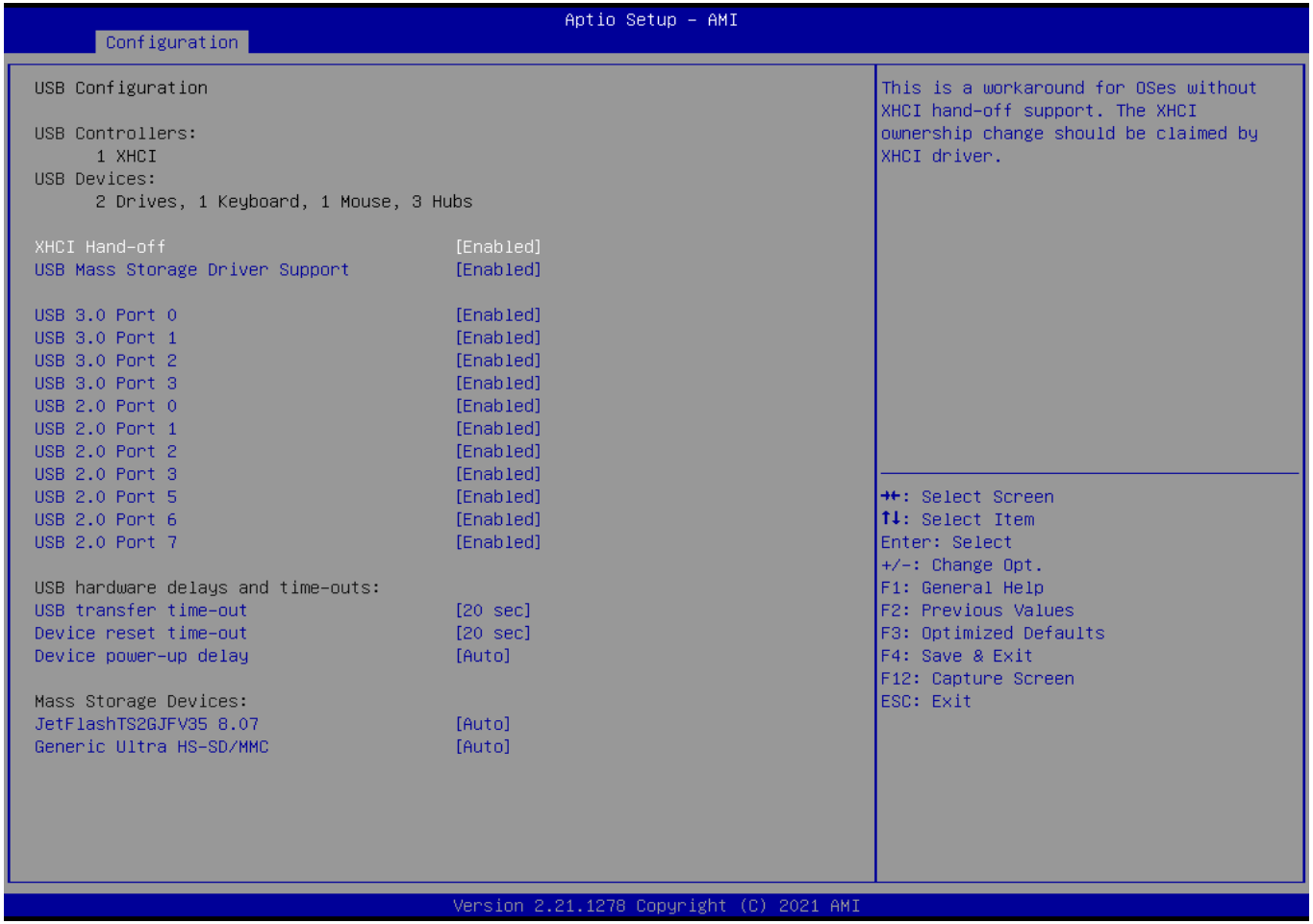
SATA Configuration



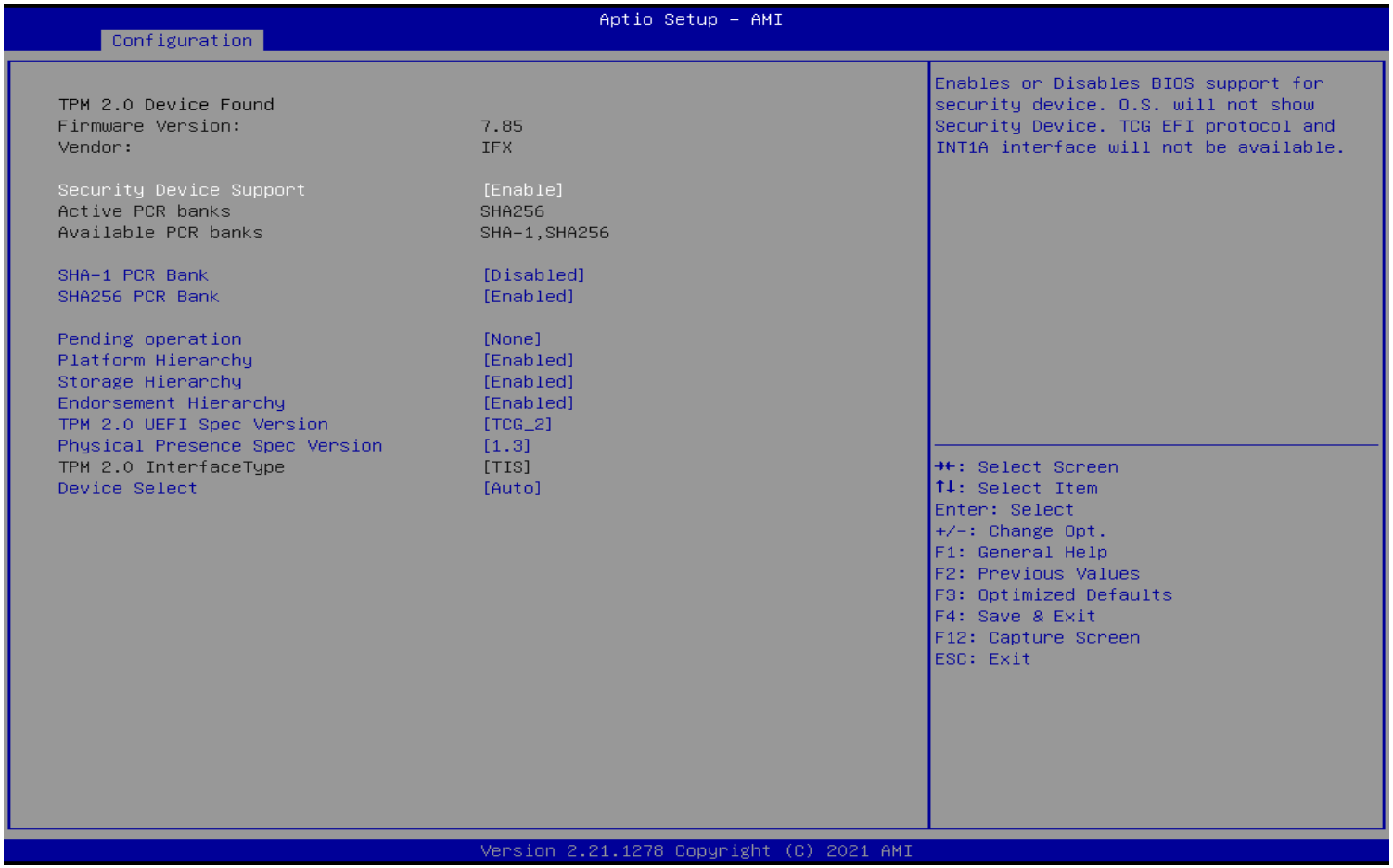
Feature	Description	Options
Serial ATA Port 0		
Port 0	Enabled or Disabled SATA Port	★ Enabled , Disabled
Hot plug	Designates this port as Hot pluggable.	★ Disabled, Enabled
SATA Device Type	Identify the SATA port is connected to Solid State Drive or Hard Disk Drive.	★ Hard Disk Drive, Solid State Drive
Serial ATA Port 1		
Port 1	Enabled or Disabled SATA Port	★ Enabled , Disabled
Hot plug	Designates this port as Hot pluggable.	★ Disabled, Enabled
SATA Device Type	Identify the SATA port is connected to Solid State Drive or Hard Disk Drive.	★ Hard Disk Drive, Solid State Drive
Mini-PCIe & mSATA Switch	Select Slot (J17) to be mSATA or Mini PCIe. [Auto] will use Pin7 to detect device type.	★ mSATA , Mini PCIe, Auto

USB Configuration



Feature	Description	Options
XHCI Hand-off	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.	★ Enabled , Disabled
USB Mass Storage Driver Support	Enable/Disable USB Mass Storage Driver Support.	★ Enabled , Disabled
COMe USB 3.0 Port 0 ~ 3	Enable/Disable this USB Physical Connector (physical port). Once disabled, any USB device plug into the connector will not be detected by BIOS or OS.	★ Enabled , Disabled
COMe USB 2.0 Port 0 ~ 7	Enable/Disable this USB Physical Connector (physical port). Once disabled, any USB device plug into the connector will not be detected by BIOS or OS.	★ Enabled , Disabled
USB transfer time-out	The time-out value for Control, Bulk, and Interrupt transfers.	★ 20 sec , 1, 5, 10
Device reset time-out	USB mass storage device Start Unit command time-out.	★ 20, 10, 30, 40 sec
Device power-up delay	Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port it is 100 ms, for a Hub port the delay is taken from Hub descriptor.	★ Auto, Manual
Device power-up delay -- ★ Manual		
Device power-up delay in seconds	Delay range is 1..40 seconds, in one second increments	★ 5
Generic Ultra HS-SD/MMC	Mass storage device emulation type. 'AUTO' enumerates devices according to their media format. Optical drives are emulated as 'CDROM'; drives with no media will be emulated according to a drive type.	★ Auto, Floppy, Forced FDD, Hard Disk, CD-ROM

TPM 2.0 Device Found



Feature	Description	Options
Security Device Support	Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A Interface will not be available.	★ Enabled, Disabled
SHA-1 PCR Bank	Enables or Disables SHA-1 PCR Bank.	★ Disabled, Enabled
SHA256 PCR Bank	Enables or Disables SHA256 PCR Bank.	★ Enabled, Disabled
Pending operation	Schedule an Operation for the Security Device. Note: Your Computer will reboot during restart in order to change State of Security Device.	★ None, TPM Clear
Platform Hierarchy	Enables or Disables Platform Hierarchy.	★ Enabled, Disabled
Storage Hierarchy	Enables or Disables Storage Hierarchy.	★ Enabled, Disabled
Endorsement Hierarchy	Enables or Disables Endorsement Hierarchy.	★ Enabled, Disabled
TPM2.0 UEFI Spec Version	Select the TCG2 Spec Version Support. TCG_1_2: the Compatible mode for Win8/Win10. TCG_2: Support new TCG2 protocol and event format for Win10 or later.	★ TCG_2, TCG_1_2
Physical Presence Spec Version	Select to Tell O.S. to Support PPI Spec Version 1.2 or 1.3. Not some HCK tests might not support 1.3.	★ 1.3, 1.2
Device Select	TPM 1.2 will restrict support to TPM 1.2 devices, TPM 2.0 will restrict support to TPM 2.0 devices, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 devices will be enumerated.	★ Auto, TPM 1.2, TPM 2.0

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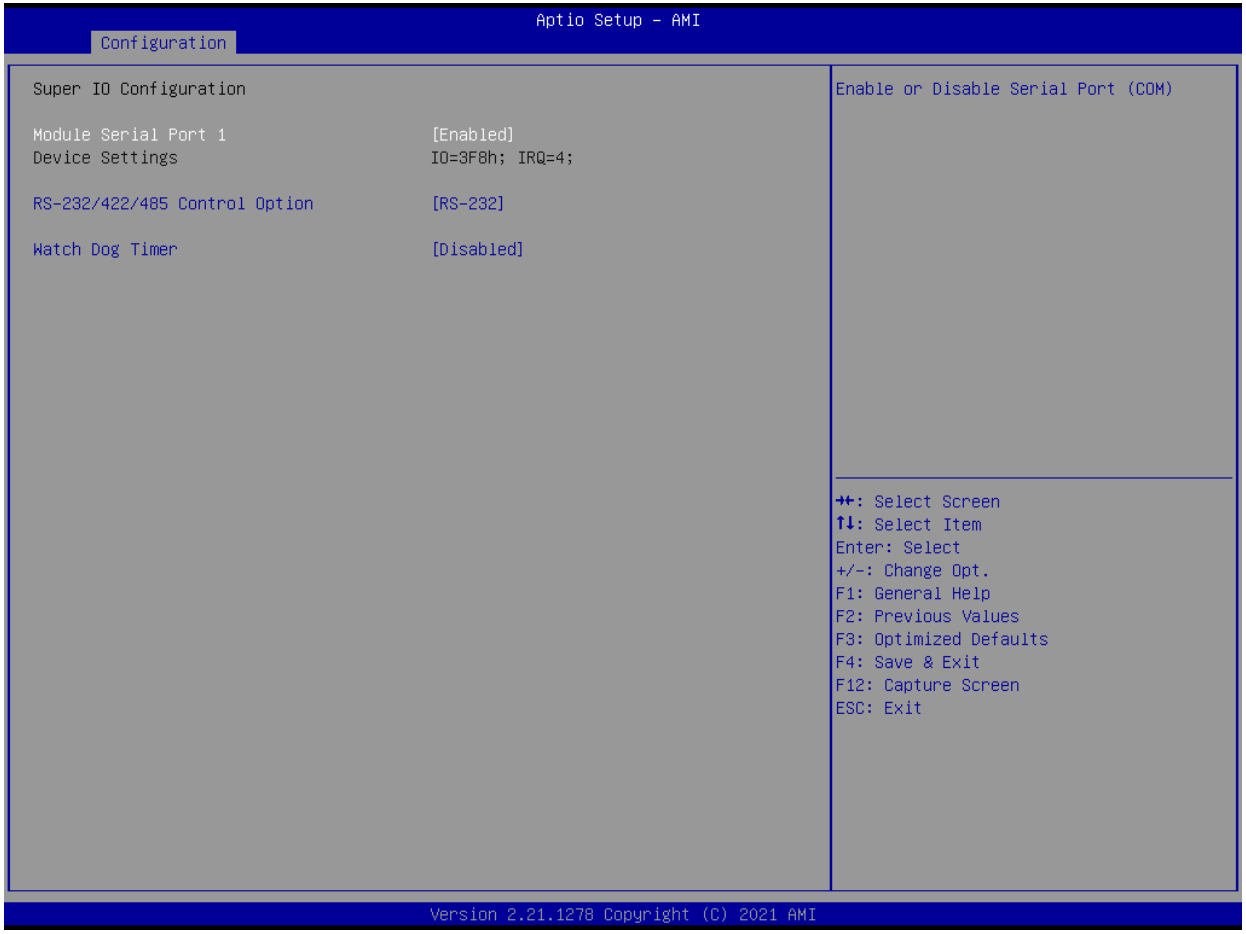
Super IO Configuration



Feature	Description	Options
Module Serial Port 1	Enable or Disable Serial Port (COM)	★ Enabled, Disabled
RS-232/422/485 Control Option	Serial Port 3 RS-232/422/485 Control Option	★ RS-232, RS-484 HALF DUPLEX, RS-422 FULL DUPLEX,
Watch Dog Timer	Enable/Disable Watch Dog Timer	★ Disabled, Enabled
Watch Dog Timer [Enabled]		
Timer Unit	Select Timer count unit of WDT [Watch Dog Timer [Enabled]]	★ Second, Minute
Timer value	Set WDT Timer value seconds / minutes [Watch Dog Timer [Enabled]]	★ 20

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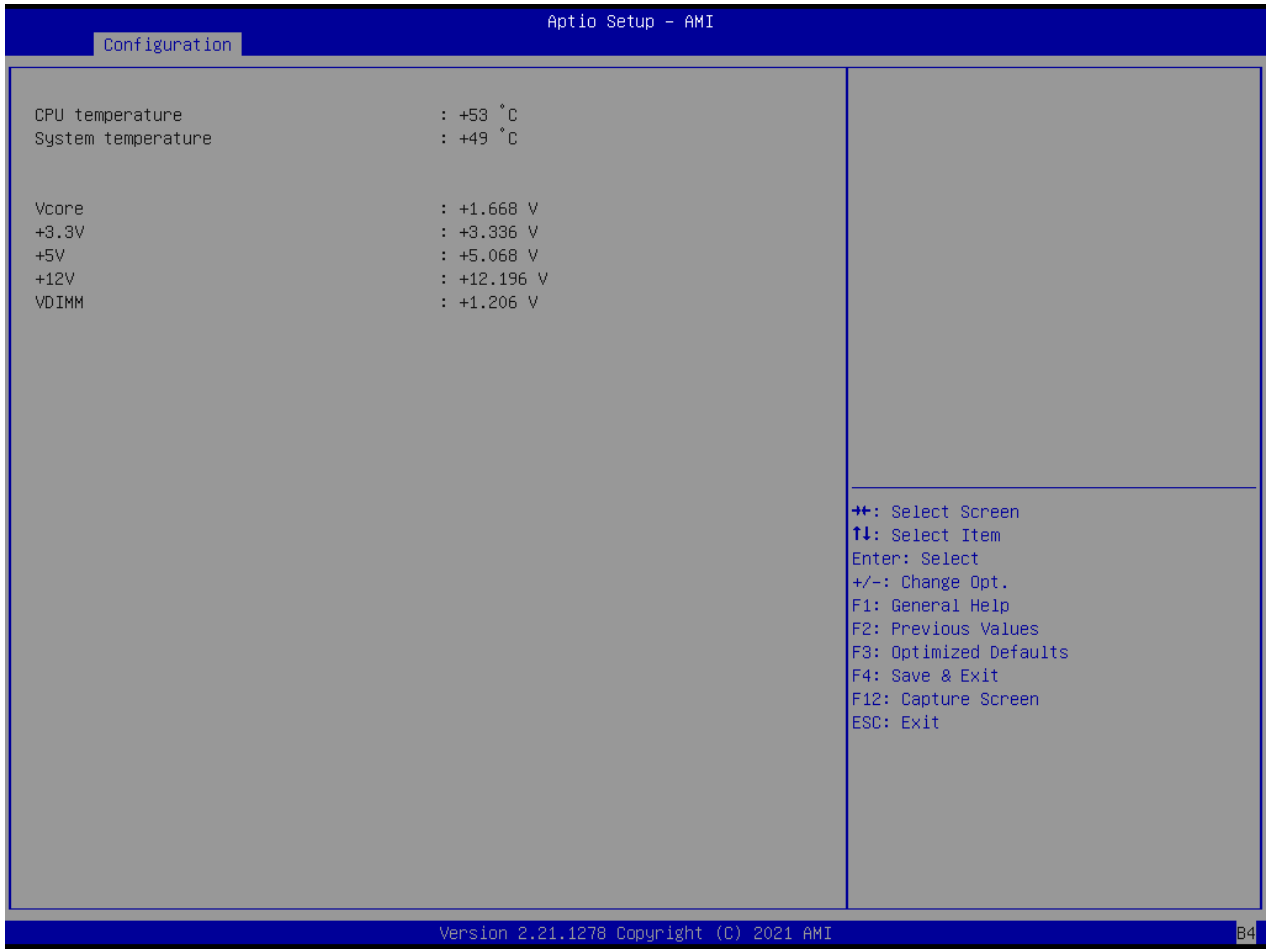
HW Monitor


Aptio Setup – AMI
Configuration
CPU temperature : +53 °C
System temperature : +49 °C
Vcore : +1.668 V
+3.3V : +3.336 V
+5V : +5.068 V
+12V : +12.196 V
VDIMM : +1.206 V
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
F12: Capture Screen
ESC: Exit
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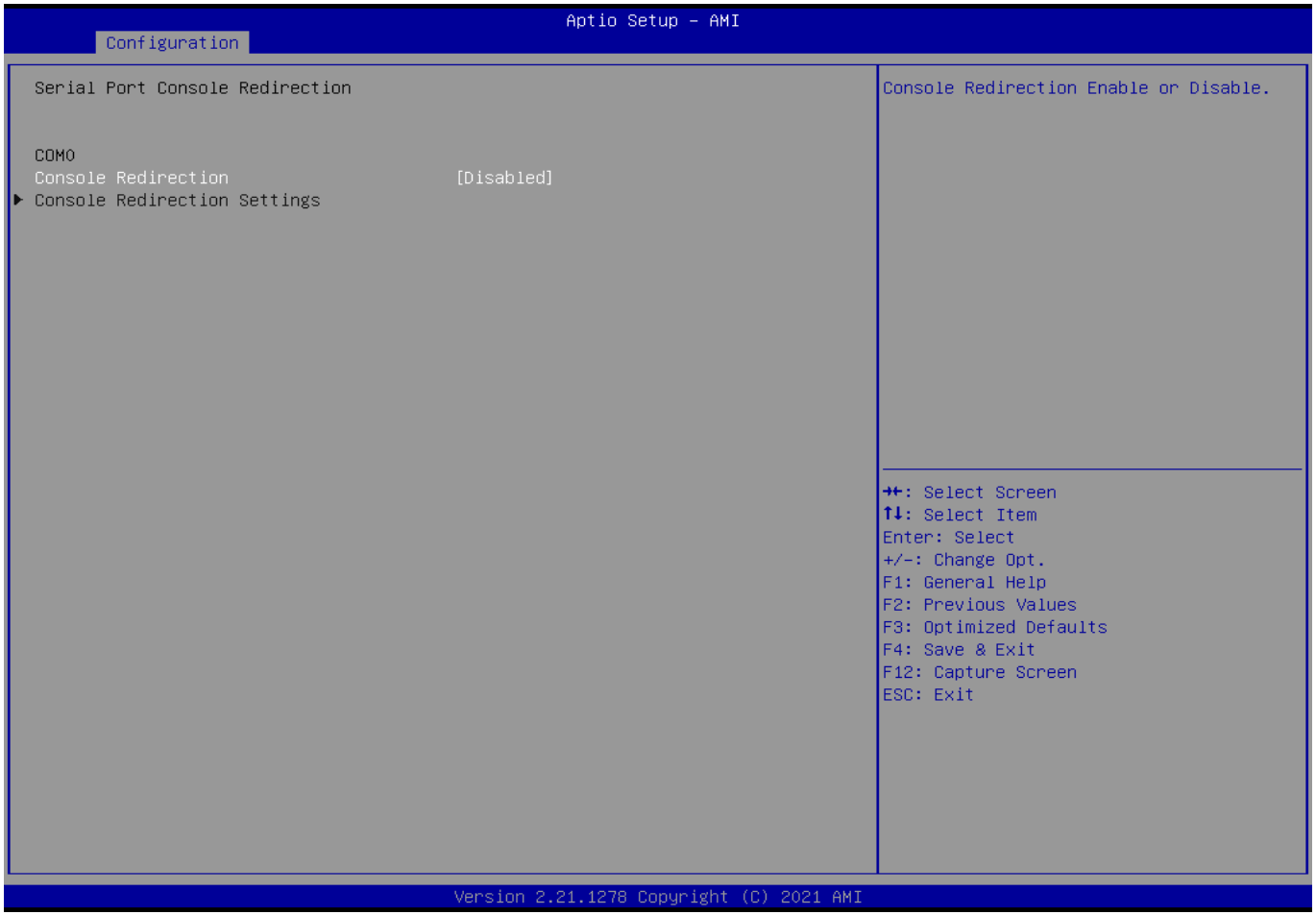
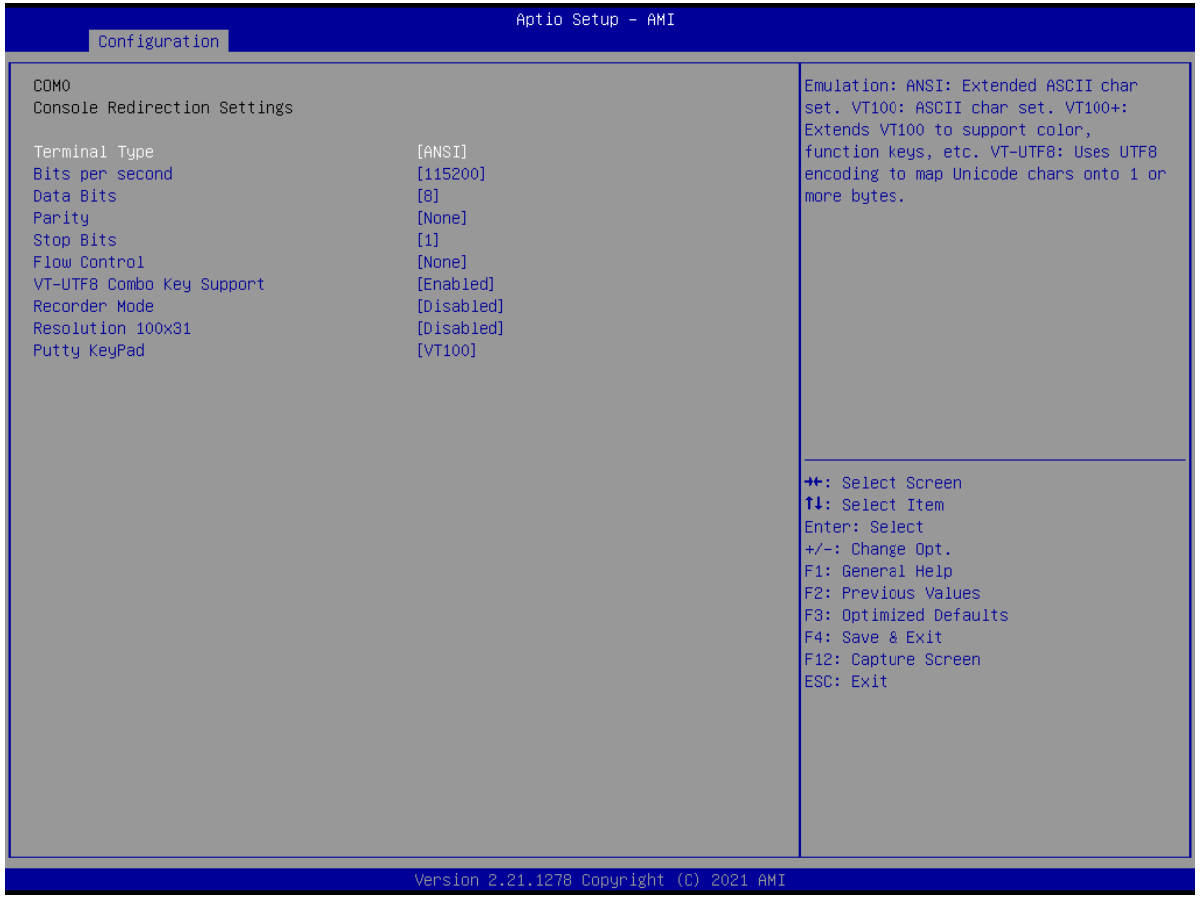
B4

Serial Port Console Redirection



Feature	Description	Options
COM0 Console Redirection	Console Redirection Enable or Disable	★ Disabled, Enabled

COM0 Console Redirection Settings:



Feature	Description	Options
Terminal Type	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.	★ ANSI, VT100, VT100+, VT-UTF8
Bits per second	Select Serial port transmission speed. The speed must be matched on other side. Long or noisy lines may require lower speeds.	★ 115200, 9600, 19200, 38400, 57600
Data bits	Data bits	★ 8, 7
Parity	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space parity bit is always 0. Mark and Space Parity do not allow for error detection. They can be used as an additional data bit.	★ None, Even, Odd, Mark, Space
Stop Bits	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.	★ 1, 2
Flow Control	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signal.	★ None, Hardware RTS/CTS
VT-UTF8 Combo Key Support	Enable VT-UTF8 Combination Key Support for ANSI / VT100 terminals	★ Enabled, Disabled
Recorder Mode	With this mode enabled only text will be sent. This is to capture Terminal data.	★ Disabled, Enabled
Resolution 100x31	Enables or disables extended terminal resolution	★ Disabled, Enabled
Putty KeyPad	Select Function Key and KeyPad on Putty.	★ VT100, LINUX, XTERMR6, SCO, ESCN, VT400

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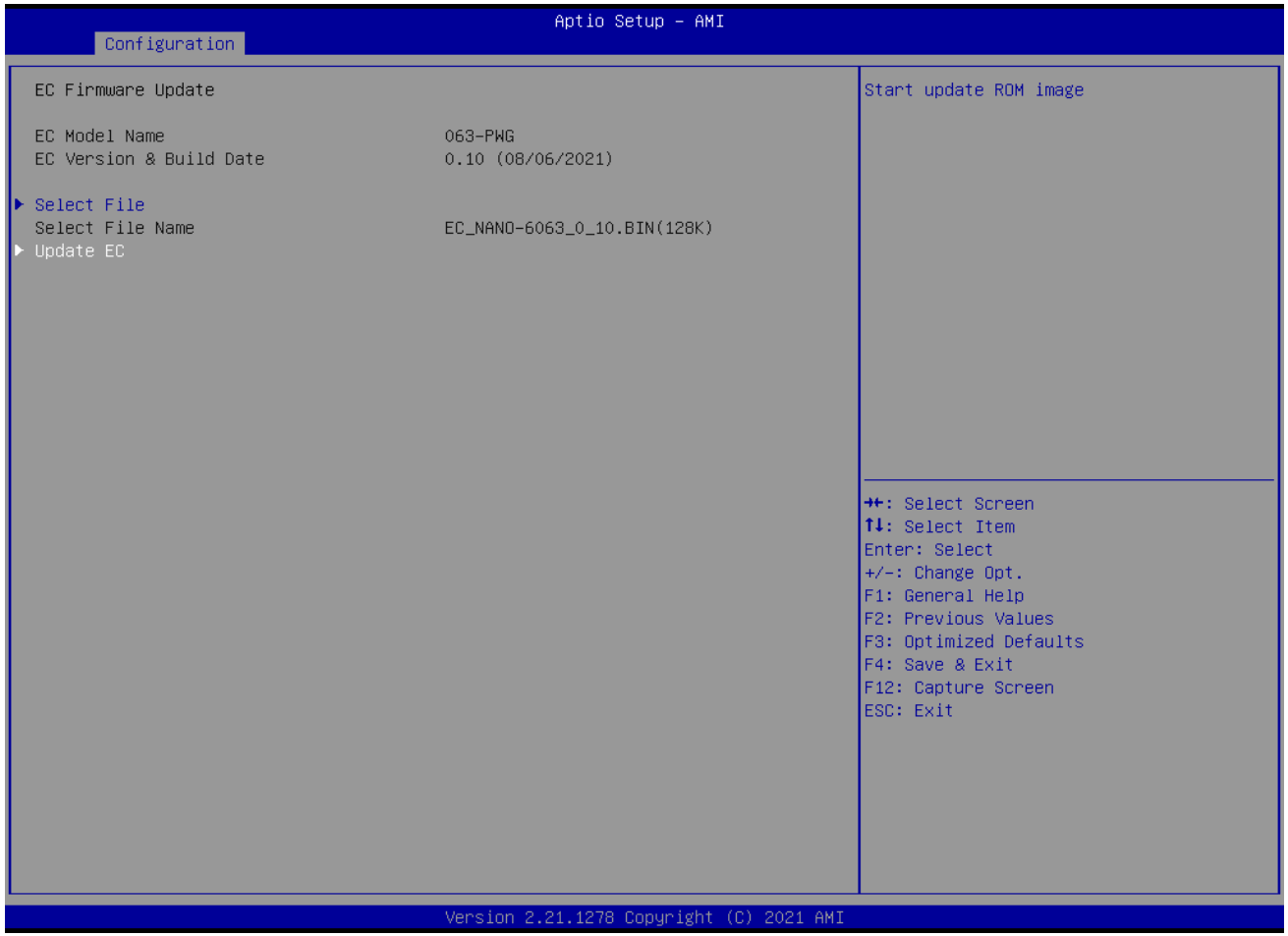
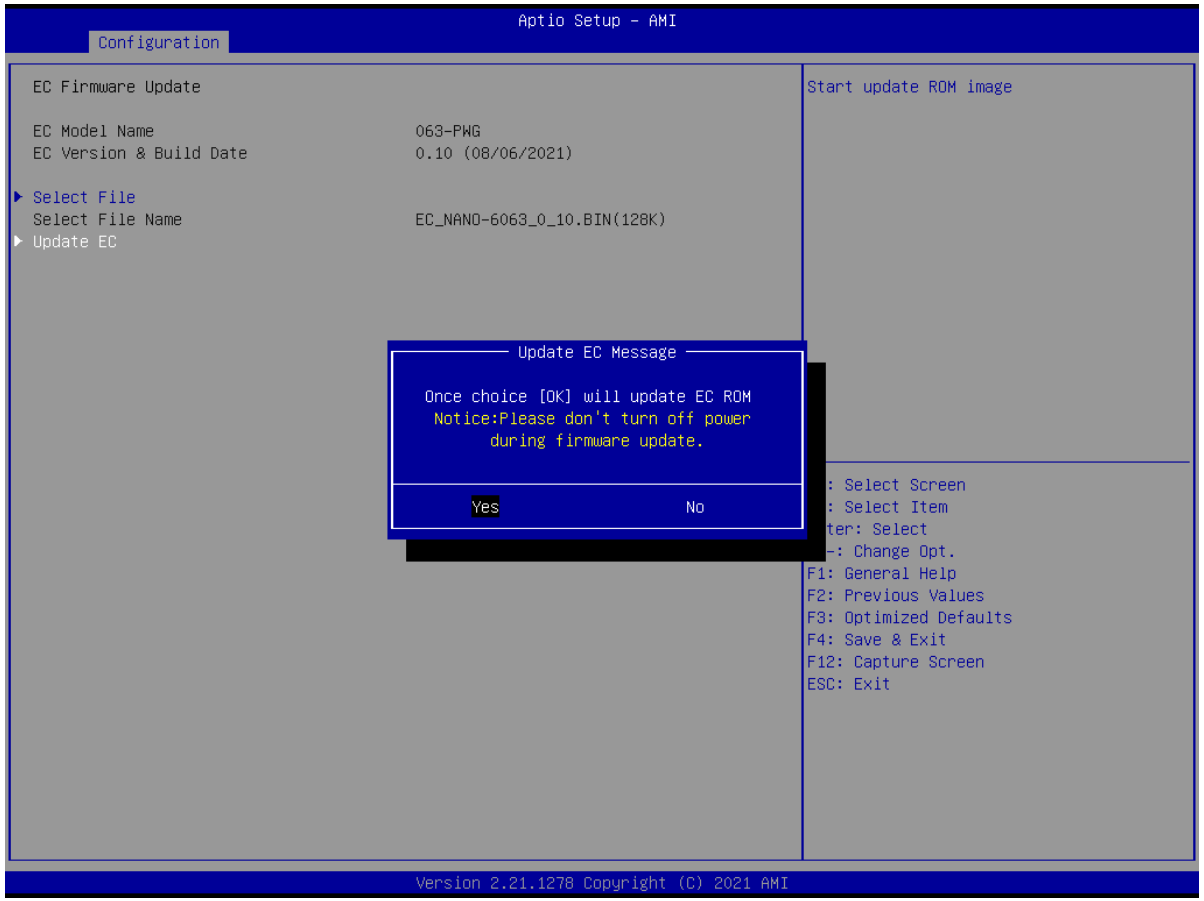
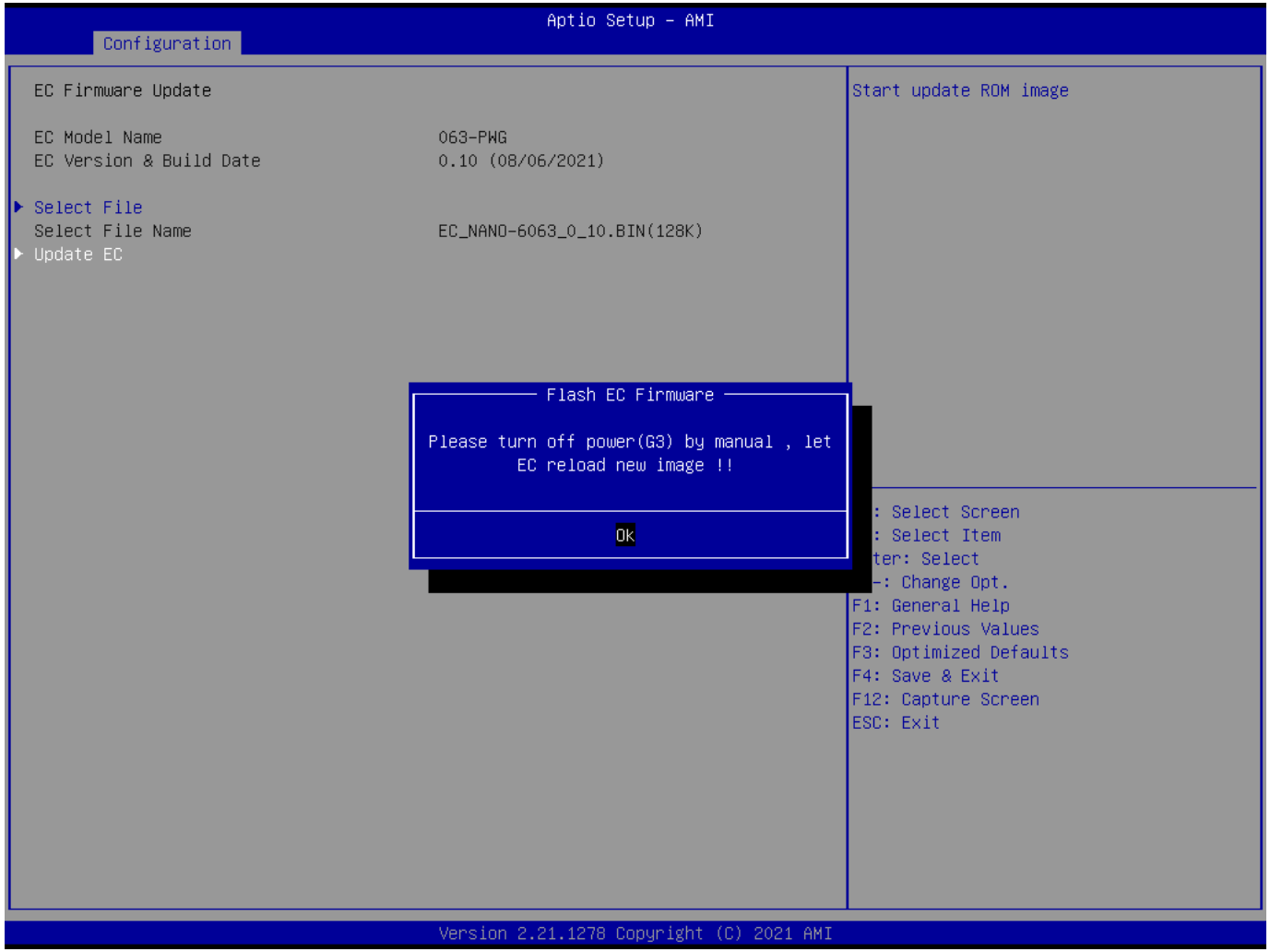
EC Firmware Update



Feature	Description	Options
Select File	Select ROM image	Bin file to the USB DOK

Update EC




Aptio Setup – AMI
Configuration
EC Firmware Update
EC Model Name 063-PWG
EC Version & Build Date 0.10 (08/06/2021)
Select File
Select File Name EC_NANO-6063_0_10.BIN(128K)
Update EC
Start update ROM image
Flash EC Firmware
Please turn off power(G3) by manual , let EC reload new image !!
Ok
: Select Screen
: Select Item
ter: Select
-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
F12: Capture Screen
ESC: Exit
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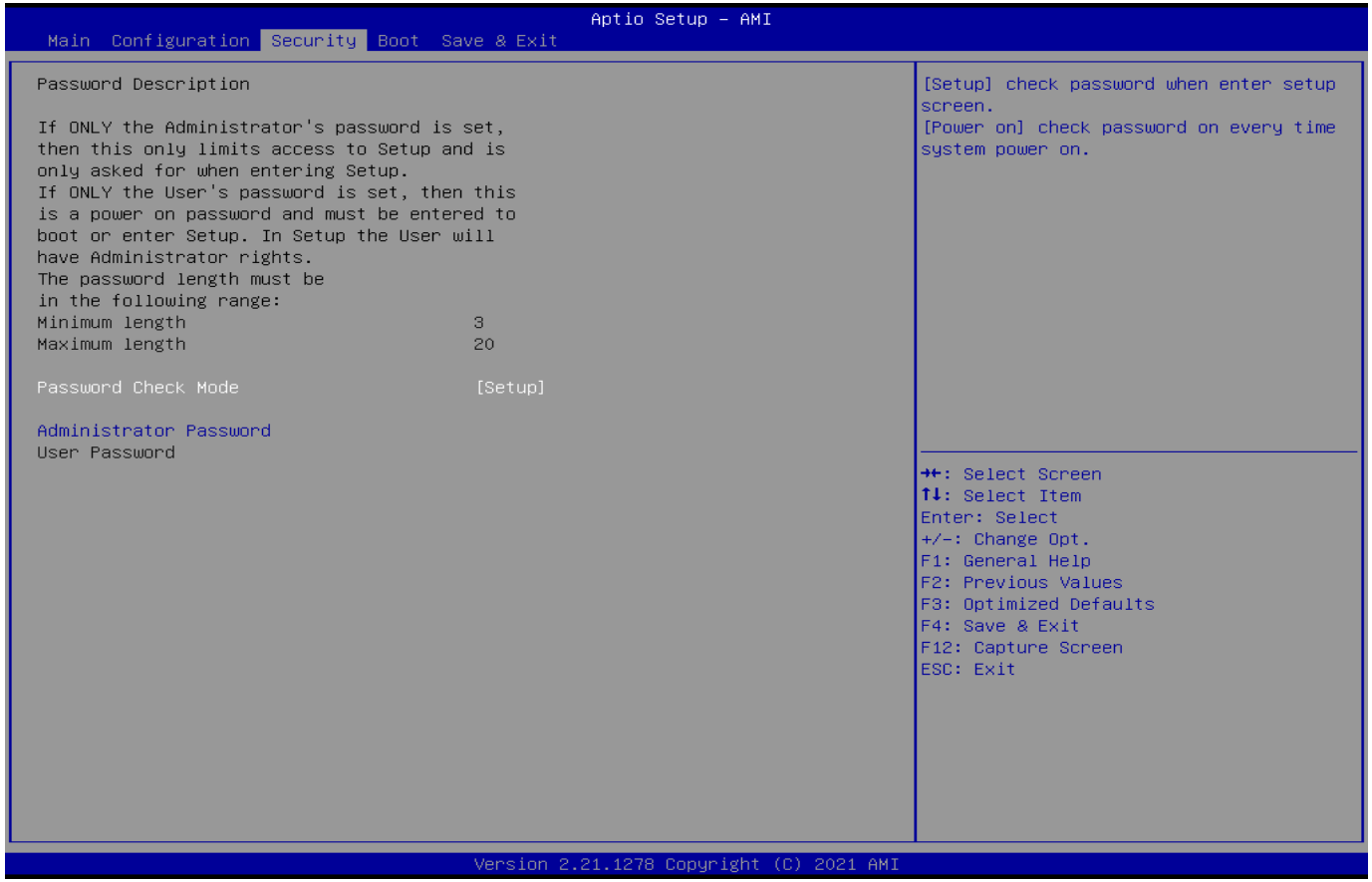
Security


Aptio Setup – AMI
Main Configuration Security Boot Save & Exit
Password Description
If ONLY the Administrator's password is set, then this only limits access to Setup and is only asked for when entering Setup.
If ONLY the User's password is set, then this is a power on password and must be entered to boot or enter Setup. In Setup the User will have Administrator rights.
The password length must be in the following range:
Minimum length 3
Maximum length 20
Password Check Mode [Setup]
Administrator Password
User Password
[Setup] check password when enter setup screen.
[Power on] check password on every time system power on.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
F12: Capture Screen
ESC: Exit
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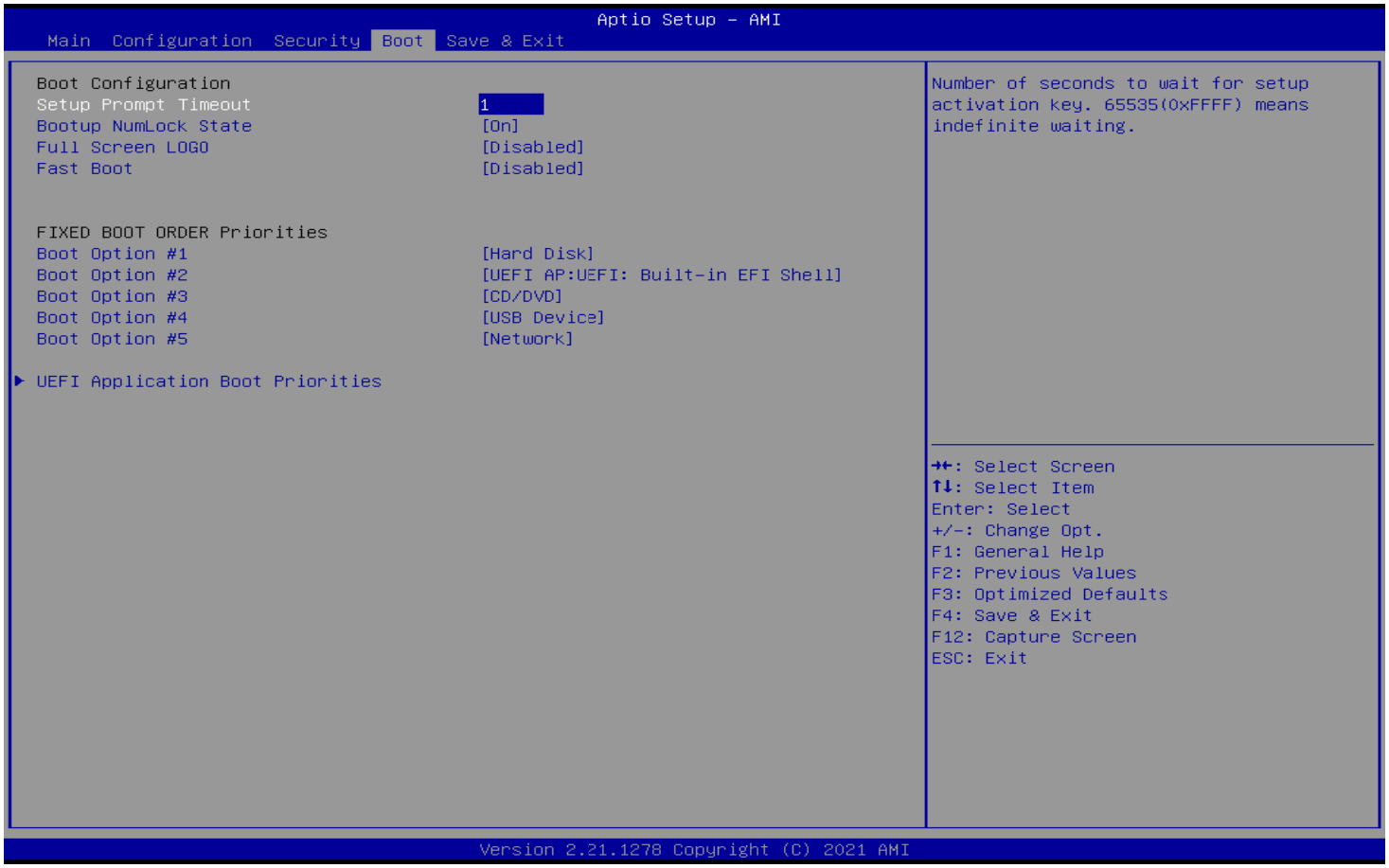
Feature	Description	Options
Password Check Mode	[Setup] check password when enter setup screen. [Power on] check password on every time system power on.	★ Setup, Power On
Administrator Password	Set Administrator Password	

Boot


Aptio Setup – AMI
Main Configuration Security Boot Save & Exit
Boot Configuration
Setup Prompt Timeout 1
Bootup NumLock State [On]
Full Screen LOGO [Disabled]
Fast Boot [Disabled]
FIXED BOOT ORDER Priorities
Boot Option #1 [Hard Disk]
Boot Option #2 [UEFI AP:UEFI: Built-in EFI Shell]
Boot Option #3 [CD/DVD]
Boot Option #4 [USB Device]
Boot Option #5 [Network]
UEFI Application Boot Priorities
Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
F12: Capture Screen
ESC: Exit
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Feature	Description	Options
Setup Prompt Timeout	Set the default timeout before system boot. A value of 65535 will disable the timeout completely.	★ 1
Bootup NumLock State	Select the keyboard NumLock state.	★ On, Off
Full Screen LOGO	Enables or disables Quiet Boot option and Full screen Logo.	★ Disabled, Enabled
Fast Boot	Enables or disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options.	★ Disabled, Enabled
Boot Option #1 ~ #5	Sets the system boot order	Hard Disk, UEFI AP: UEFI: Built-in EFI Shell, CD/DVD, USB Device; Network, Disabled
UEFI Application Boot Priorities	Specifies the Boot Device Priority sequence from available UEFI Application	

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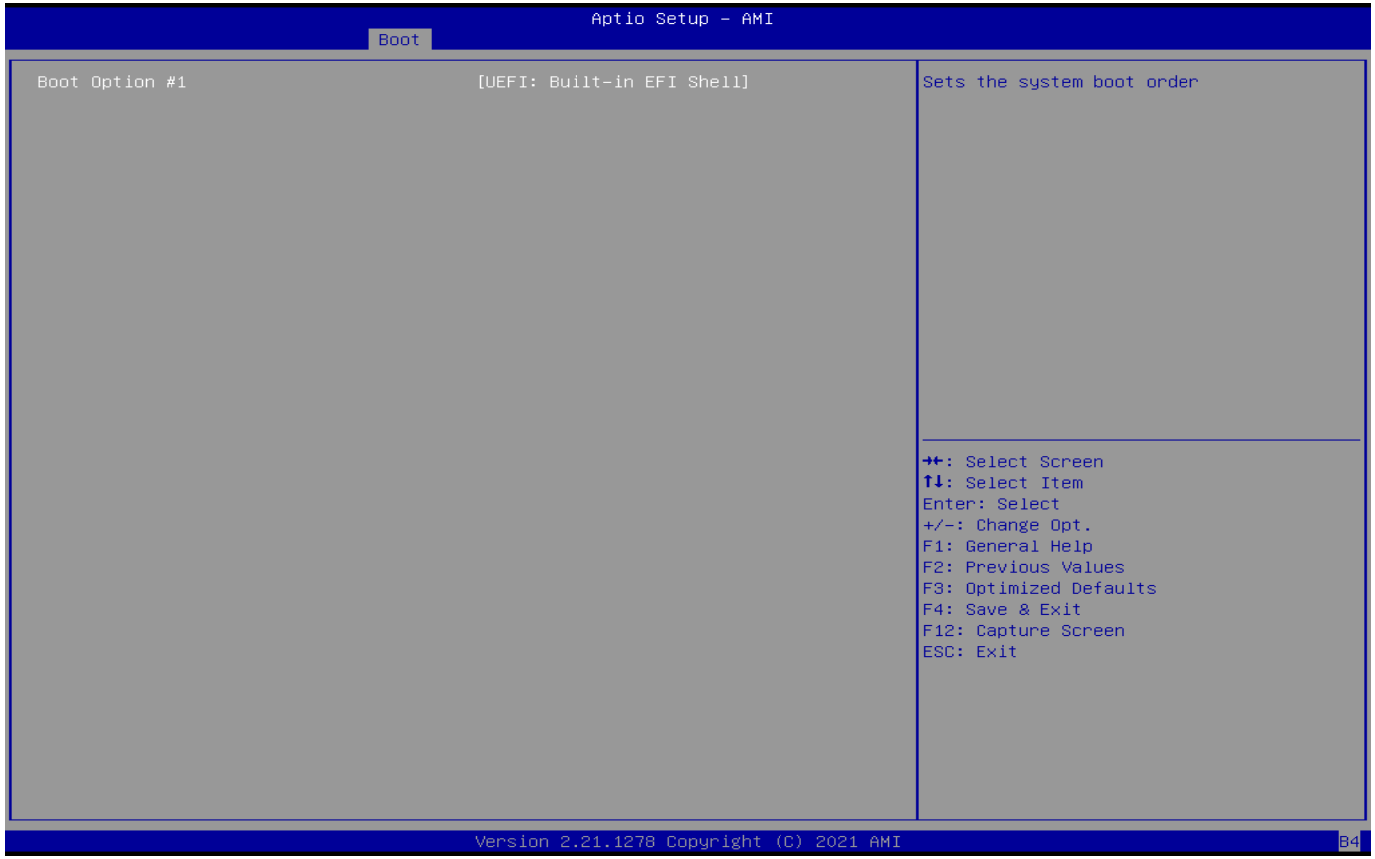
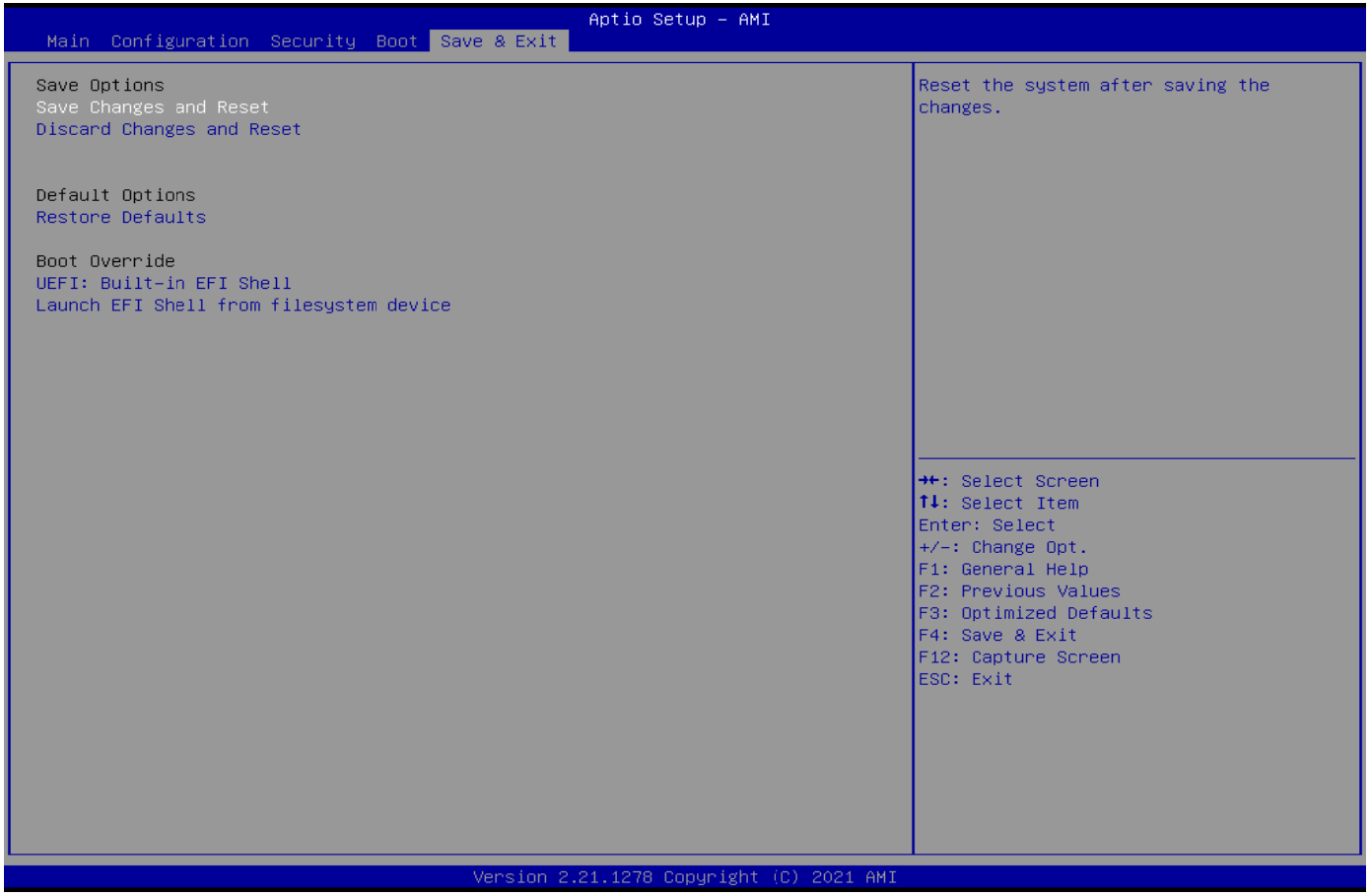
UEFI Application Boot Priorities:



Save & Exit


Aptio Setup – AMI
Main Configuration Security Boot Save & Exit
Save Options
Save Changes and Reset
Discard Changes and Reset
Default Options
Restore Defaults
Boot Override
UEFI: Built-in EFI Shell
Launch EFI Shell from filesystem device
Reset the system after saving the changes.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
F12: Capture Screen
ESC: Exit
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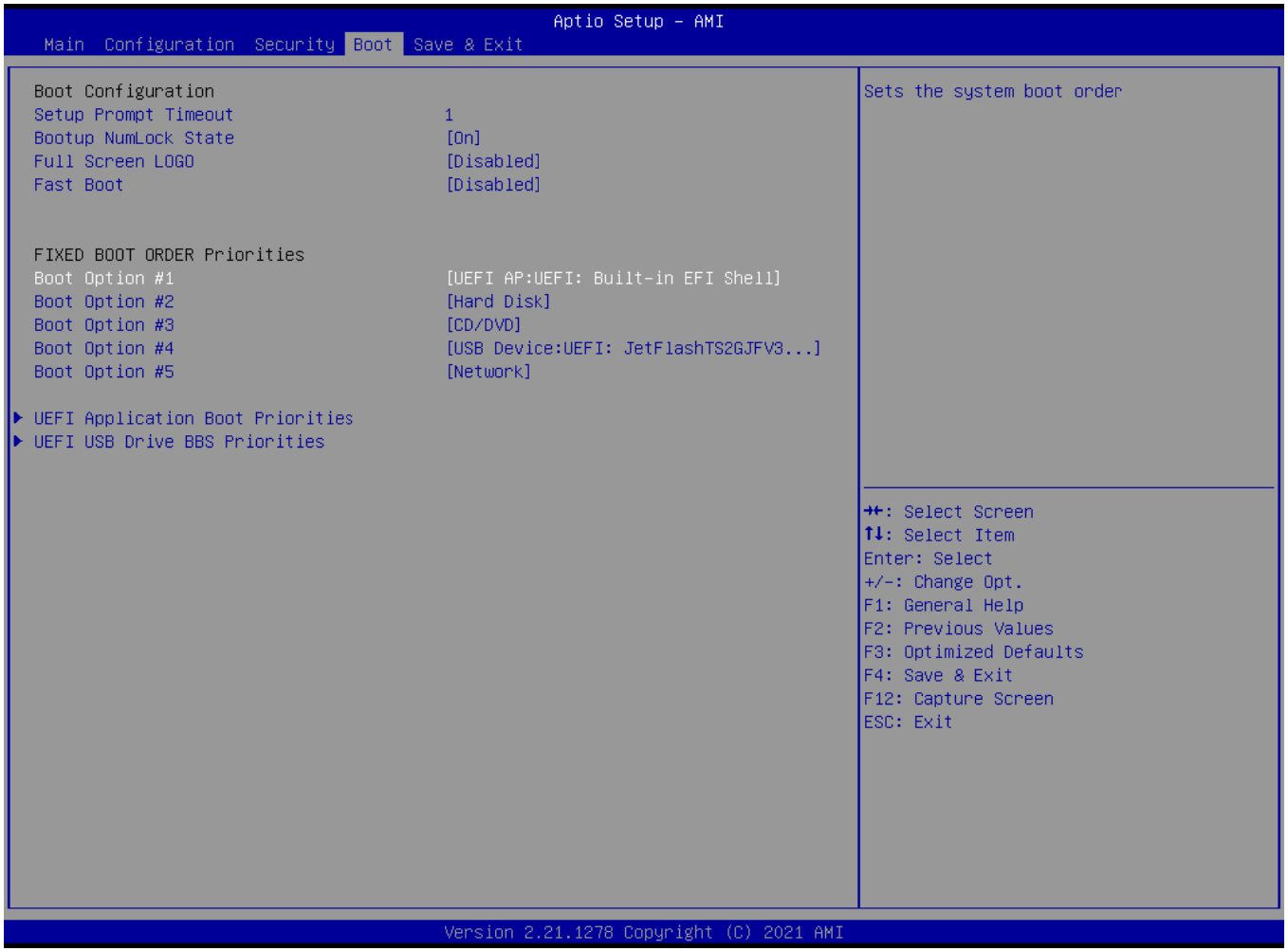
Feature	Description	Options
Save Changes and Reset	Reset the system after saving the changes.	
Discard Changes and Reset	Reset system setup without saving any changes.	
Restore Defaults Values	Restore/Load Default values for all the setup options.	
UEFI: Built-in EFI Shell	Reset the system after saving the changes. (Boot option filter: UEFI only)	

NANO-6063 BIOS / EC UEFI Update SOP process

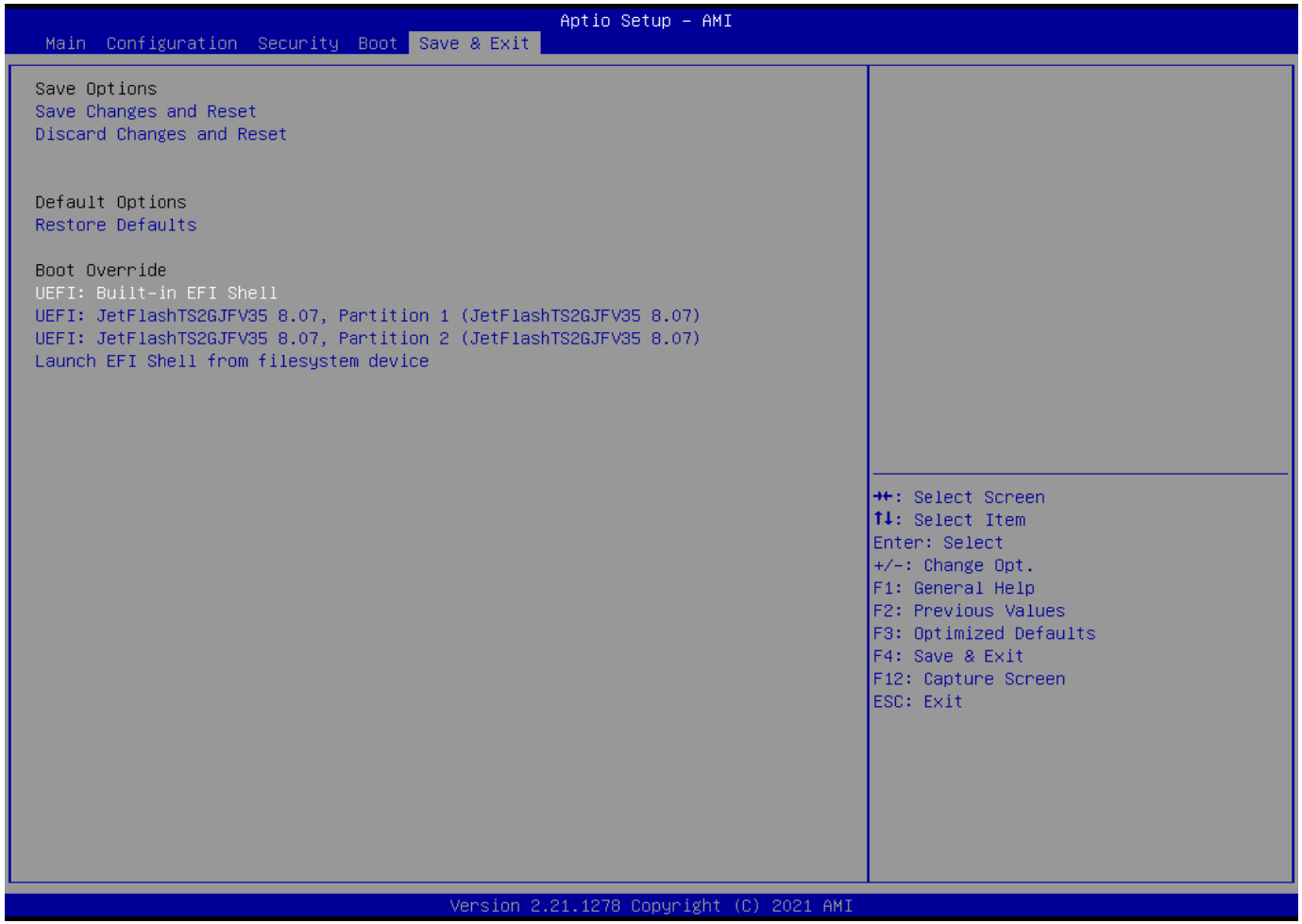
Step 1. Prepare a USB DOK.

Step 2. Unzip update file to the USB DOK.

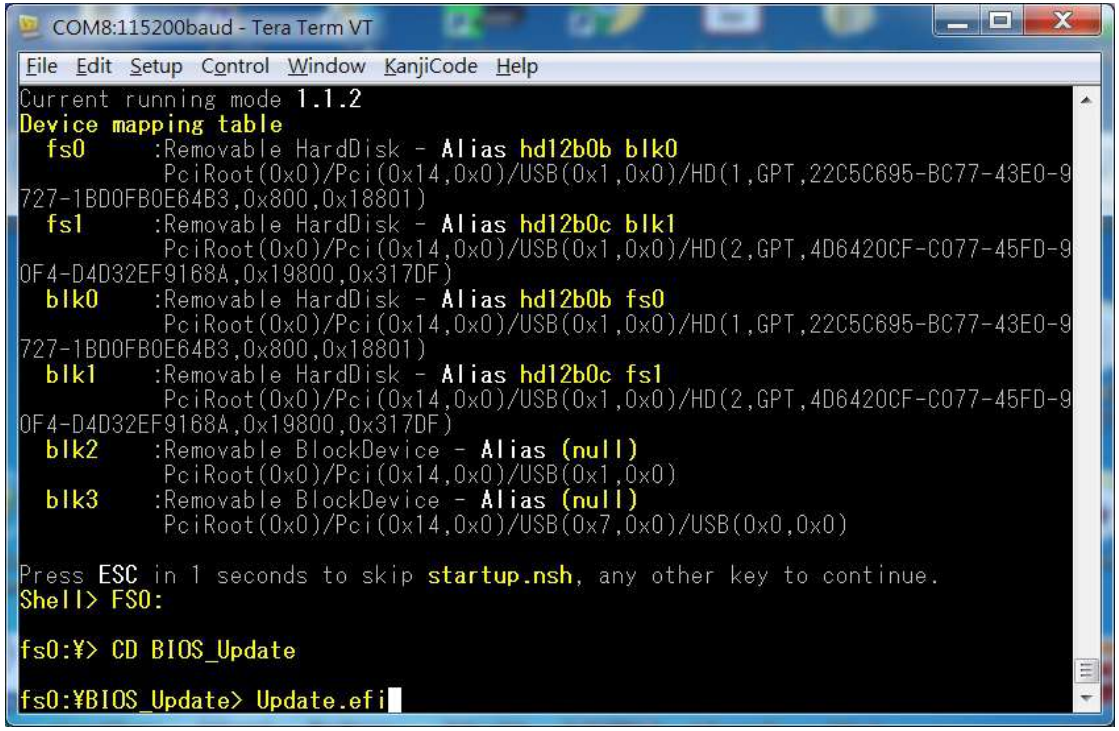
Step 3. Select UEFI: Built-in EFI Shell in the BIOS boot menu and save then restarts the system.


Aptio Setup – AMI
Main Configuration Security Boot Save & Exit
Boot Configuration
Setup Prompt Timeout 1
Bootup NumLock State [On]
Full Screen LOGO [Disabled]
Fast Boot [Disabled]
FIXED BOOT ORDER Priorities
Boot Option #1 [UEFI AP:UEFI: Built-in EFI Shell]
Boot Option #2 [Hard Disk]
Boot Option #3 [CD/DVD]
Boot Option #4 [USB Device:UEFI: JetFlashTS2GJFV3...]
Boot Option #5 [Network]
UEFI Application Boot Priorities
UEFI USB Drive BBS Priorities
Sets the system boot order
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
F12: Capture Screen
ESC: Exit
Version 2.21.1278 Copyright (C) 2021 AMI

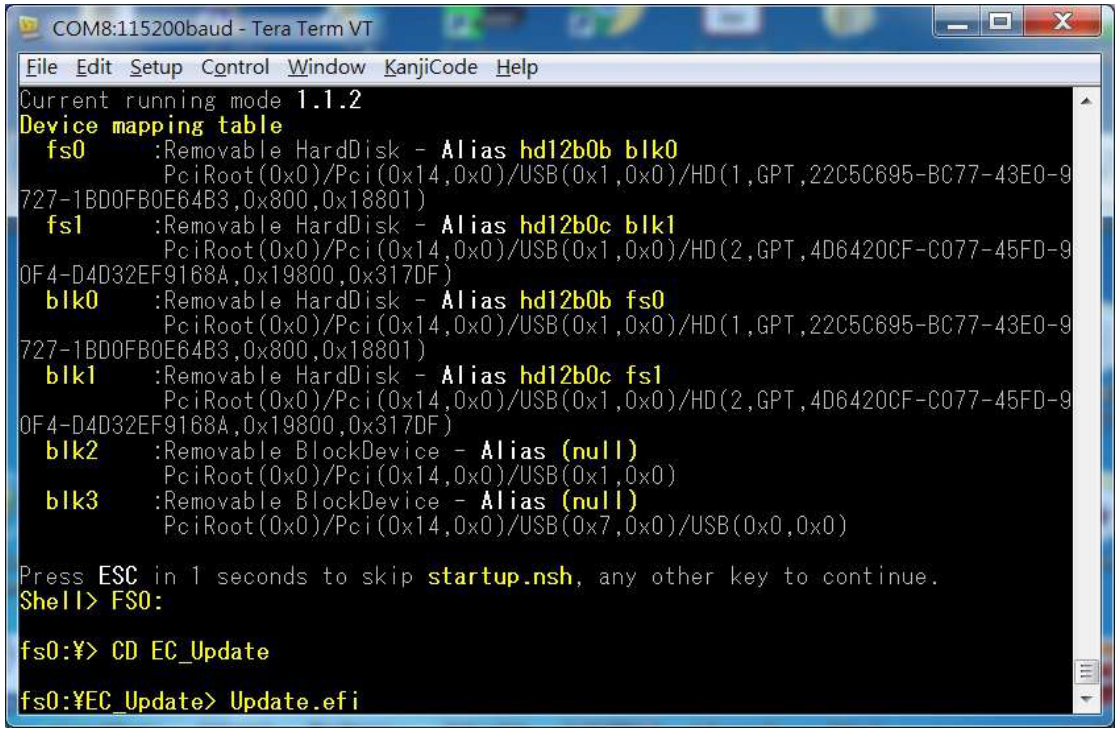
Step 4. Plug the USB DOK into the target system and boot from UEFI Shell.



Step 5. Under the UEFI shell, direct to your USB DOK, below is an example uses fs0. Then direct to the folder with updated file and type command: "update" and press enter.

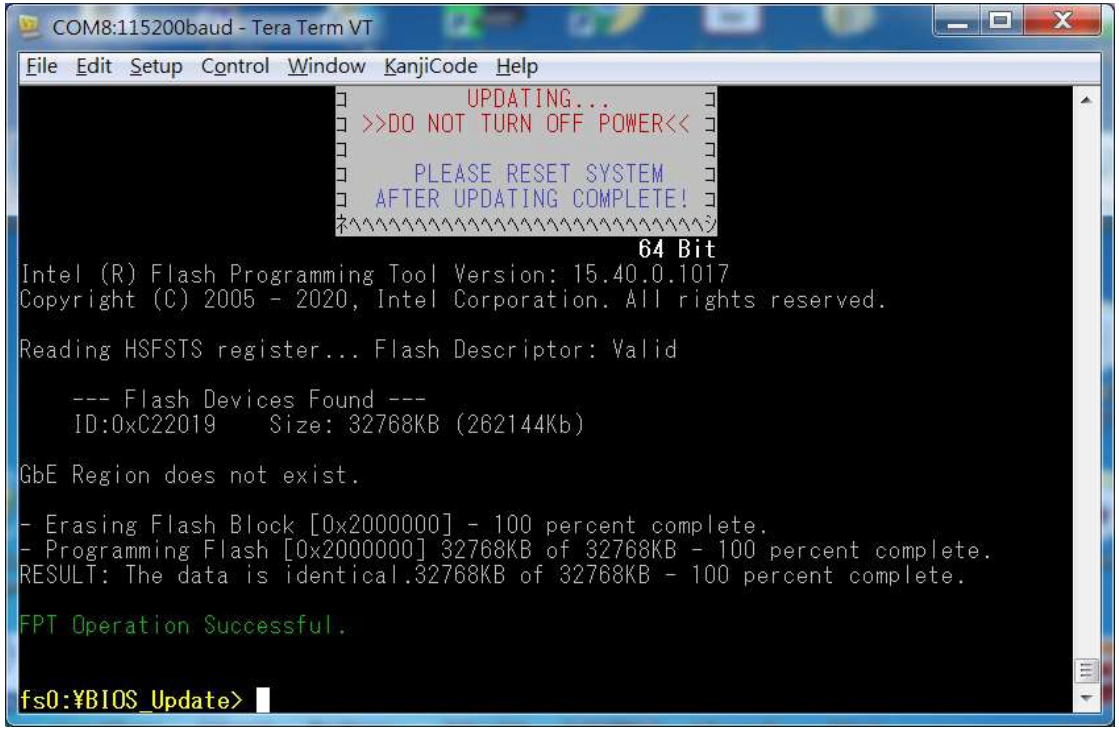


(BIOS File Update)

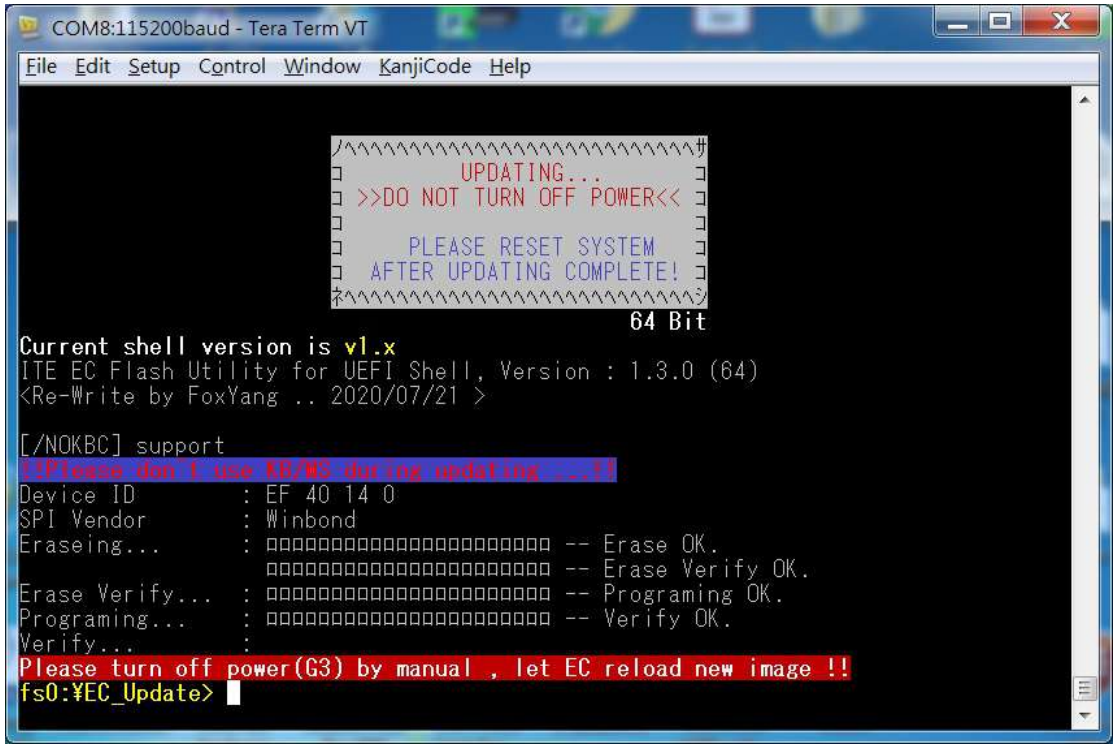


(EC File Update)

Step 6. The updating process will start and you can see the updating progress. Once finished, please power off and restart the system.



(BIOS updating progress)



(EC updating progress)

7 System Resources

7.1 Intel®Elkhart LakeSoC

Intel Atom® x6211E Processor(1.5M Cache, up to 3.0 GHz)
Intel Atom® x6413E Processor(1.5M Cache, up to 3.0 GHz)
Intel Atom® x6425E Processor(1.5M Cache, up to 3.0 GHz)
Intel Atom® x6425RE Processor(1.5M Cache, up to 1.9 GHz)

7.2 Main Memory

NANO-6063 provides 1 x 260-pin SO-DIMM sockets which supports DDR4 non-ECC memory. The maximum memory can be up to 32GB. Memory clock and related settings can be detected by BIOS via SPD interface.

Watch out the contact and lock integrity of memory module with socket, it will impact on the system reliability. Follow normal procedures to install memory module into memory socket. Before locking, make sure that all modules have been fully inserted into the card slots.

7.3 Installing the Single Board Computer

To install your NANO-6063 into standard chassis or proprietary environment, please perform the following:
Step 1 : Check all jumpers setting on proper position
Step 2 : Install and configure memory module on right position
Step 3 : Place NANO-6063 into the dedicated position in the system
Step 4 : Attach cables to existing peripheral devices and secure it

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WARNING

Please ensure that motherboard is properly inserted and fixed by mechanism.

Note:

Please refer to section 6.3.1 to 6.3.4 to install INF/Graphic/LAN

7.3.1 Chipset Component Driver

The NANO-6063 build with Intel Atom® processor x6000E series. It's a new chipset that some old operating systems might not be able to recognize. To overcome this compatibility issue, for Windows Operating Systems such as Windows 8, please install its INF before any of other Drivers are installed. You can find very easily this chipset component driver in NANO-6063 CD-title

7.3.2 Intel® Gen 11 HD Graphics

NANO-6063 has integrated Intel® Gen 11 HD Graphics. Processor Graphics indicates graphics processing circuitry integrated into the processor, providing the graphics, compute, media, and display capabilities.

NANO-6063 supports HDMI, DP,VGA display output. This combination makes NANO-6063 an excellent performance hardware.

Drivers Support

The driver supports Windows 10.

8 Troubleshooting

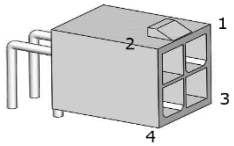
This chapter provides a few useful tips to quickly get NANO-6063 running with success. As basic hardware installation has been addressed in Chapter 2, this chapter will focus on system integration issues, in terms of BIOS setting, and OS diagnostics.

8.1 Hardware Quick Installation

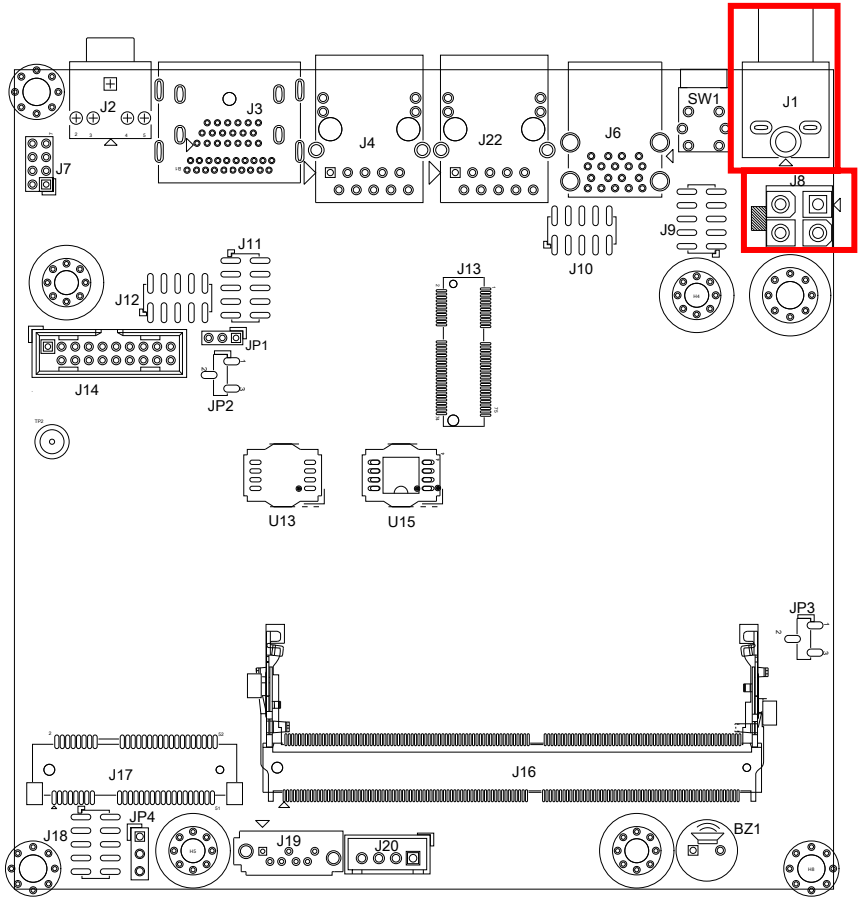
ATX Power Setting

There are two methods to connect the power of NANO-6063 which are 12V DC Jack (J1) & 4 Pins 12V DC input (J8). It's able to be chosen either one for NANO-6063.

J8: ATX 4 Pin Connector

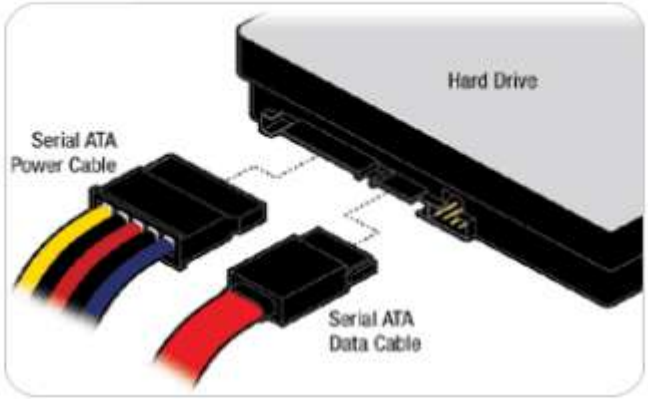


PIN No.	Signal Description
1	+12V
2	+12V
3	Ground
4	Ground


J1
J2
J3
J4
J6
J7
J8
J9
J10
J11
J12
J13
J14
JP1
JP2
JP3
JP4
J16
J17
J18
J19
J20
SW1
BZ1
U13
U15

Serial ATA

Serial ATA Hard Disk Setting for SATA Speed Selection



System BIOS Main Menu

Configuration

SATA Configuration ..... [Press enter]

SATA Speed Selection [Auto, Gen1, Gen2, Gen3]

8.2 BIOS Setting

It is assumed that users have correctly adopted modules and connected all the devices cables required before turning on ATX power.
260-pin DDR4 3200MT/sSO-DIMM Memory, keyboard, mouse, SATA hard disk, VGA connector, device power cables, ATX accessories are good examples that deserve attention. With no assurance of properly and correctly accommodating these modules and devices, it is very possible to encounter system failures that result in malfunction of any device.

To make sure that you have a successful start with NANO-6063, it is recommended, when going with the boot-up sequence, to hit “F2” key and enter the BIOS setup menu to tune up a stable BIOS configuration so that you can wake up your system far well.

Loading the default optimal setting

When prompted with the main setup menu, please scroll down to “RestoreDefaults”, press “Enter” and select “Yes” to load default optimal BIOS setup. This will force your BIOS setting back to the initial factory configurations. It is recommended to do this so you can be sure the system is running with the BIOS setting that Portwell has highly endorsed. As a matter of fact, users can load the default BIOS setting at any time when system appears to be unstable in boot up sequence.

8.3 FAQ

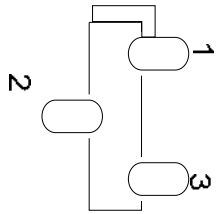
Information & Support

Question: I forgot my password of system BIOS, what am I supposed to do?

Answer: You can switch off your power supply then find the JP3 on the NANO-6063 to set it from 1-2 short to 2-3 short and wait 5 seconds to clean your

password then set it back to 1-2 short to switch on your power supply.

JP3 : CMOS Clear



PIN No.	Signal Description
1-2 Short	Clear CMOS
2-3 Short	n/a

Question: How to update the BIOS file of NANO-6063?

Answer: 1. Please visit web site ofPortwell download centeras below hyperlink
http://www.portwell.com.tw/support/download_center.php

Registering an account in advance is a must. (The E-Mail box should be an existing Company email address that you check regularly.)
http://www.portwell.com.tw/member/newmember.php

2. Type in your User name and password and log in the download center.
3. Select “Search download” and type the keyword “NANO-6063”.
4. Find the “BIOS “page and download the ROM file and flash utility.
5. Unzip file to bootable USB flash drive which can boot to shell mode. Then execute the “update.efi ”. It will start to update BIOS.
6. When you see the “FPT Operation Passed” message, which means the BIOS update processes finished. Please cut the AC power off and wait for 10 seconds before powering on.

http://www.portwell.com.tw/support/download_center.php
If you have other additional technical information or request which is not covered in this manual, please fill in the technical request form as below hyperlink.
http://www.portwell.com.tw/support/problem_report.php
We will do our best to provide a suggestion or solution for you.
Thanks

9 Portwell Software Service

Portwell Evaluation Tool (PET)

The Portwell Evaluation Tool (PET) is an API which Portwell's customers can access the GPIO, I2C, SMBus, etc under Windows and Linux OS. For more information please contact Portwell.

Portwell BIOS web Tool (PBT)

The Portwell BIOS web Tool (PBT) is a brand new on-line utility which innovated by Portwell. PBT now is available for Portwell's premiere customers who are able to add customized BIOS logoandchange BIOS default settings on American Megatrends (AMI) BIOS. Please contact Portwell for more information.

Portwell EC Auto Test Tool (PECAT)

The Portwell EC Auto Test Tool (PECAT) is a brand new utility which innovated by Portwell. PECAT now is available for Portwell's premiere customers, who are able to Test Embedded Controller Function in UEFI Mode. Please contact Portwell for more information.

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10 Industry Specifications

The list below provides links to industry specifications that apply to Portwell modules.

Low Pin Count Interface Specification, Revision 1.0 (LPC)http://www.intel.com/design/chipsets/industry/lpc.htm
Universal Serial Bus (USB) Specification, Revision 2.0http://www.usb.org/home
PCI Specification, Revision 2.3 https://www.pcisig.com/specifications
Serial ATA Specification, Revision 3.0 http://www.serialata.org/
PCI Express Base Specification, Revision 2.0 https://www.pcisig.com/specifications

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